Cooling RE3/1 and RE4/1

Ian Crotty 20 March 2017

Power dissipation for PetiRoc with integrated TDC

Channel	Chamber	FPGA+GBT	1 station	1 YE3	Rack Power	PetiRoc Dissipation
	640	20 + 1W	18		Eff 66%	
[mW]	[watt]	[W]	[W]	[W]	[W]	[W]
3.6	2.304	21	419	839	432	1271

One Endcap Power						1271

PS efficiency definition = output/input $\text{Power}_{tot} = L_{rack} + L_{chamber}$

$P_{eff} = L_{ch}/\text{power}_{tot}$ $L_{rack} = (L_{ch}/0.66) - L_{ch}$