|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Power dissipation for PetiRoc with integrated TDC** | | | | | |  |
|  |  |  |  |  |  |  |
| Channel | Chamber | FPGA+GBT | 1 station | 1 YE3 | Rack Power | PetiRoc Dissipation |
|  | 192 | 20 + 1W | 18 |  | Eff 66% |
| [mW] | [watt] | [W] | [W] | [W] | [W] | [W] |
| 6 | 1.152 | 21 | 399 | 797 | 411 | 1208 |
|  |  |  |  |  |  |  |
| One Endcap Power | |  |  |  |  | 1208 |