**Re: 1st chamber engineering meeting LV CAEN Power**

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| **Sent:** | 21 June 2018 17:04 |
| **To:** | Ian Crotty; Anton Dimitrov; Salvatore Buontempo |
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I refined the power estimation with the following procedure :

\* On FEB V1 (cyclone 2+Petiroc+wiznet ): for 4 FEB\_V1 running at maximal rate ( no dead time, treshold under pedestal, max bandwidth), we measure 2,7A consumed on the 5V power supply

=> that gives 13W for 4 FEB\_V1

=> for 1 Petiroc +1TDC FPGA (cyclone 2) +1 wiznet , we have then 13/4=3,5W

According to the wiznet datasheet, the W5300 consumption is 250mA at 3,3V , giving around 1W.

=> we have 2,5W for 1Petiroc+1cyclone 2 TDC FPGA

According to Altera, the cyclone 5 consumption is lower to the consumption of cyclone 4 of 40%. I assume that cyclone 4 and cyclone 2 have equal consumptions at equivelent design (same technology, no advertising for this at altera)

\*considering that we put about twice more TDC channels in cyclone 5 than in cyclone 2 (because of ToT), we can consider that Petiroc+cyclone 5 TDC FPGA consumption will be around 4W (i keep 0,5W margin for the 40% instead of 50%).

Then on the final FEB, having 3 petiroc + 3 TDC FPGA , that gives a total of 12W.

\* considering that a GBT chain (GBTX+GBTIA+GBTLP) consumes 2,2W(GBTX)+0,12W (GBTIA)+0,15W (GBTLP) = 2,5W

\* considering the communication FPGA will embeds the same functions, there is no reason that  it consumes something different, then we can add 2,5W for the communication part.

That gives a total of 15W per FEB, ie half of a cassette (not that far from the 23W I roughly estimated before)

If we power the FEB at 4V (the minimal voltage to give suficient margin for the voltage regulators), this gives us a current of 3,75A per FEB. Power globally dissipated in the different voltage regulators is then 3,75\*(4-3,3)=2,7W

If we power the FEB at 5V (a higher margin for the voltage regulators), this gives us a current of 3A  per FEB. Power globally dissipated in the different voltage regulatros is then 3\*(5-3,3)=5,1W

In any case we are far from limits of a A3016 (16A/90W) and we could accept a voltage drop up to :

\*4V in case of 4V applied on FEBs, leading to a max global  resistor for the LV cable up to 4/3,75=1 ohm

\*3V in case of 5V applied on FEBs, leading to a max global  resistor for the LV cable up to 3/3=1 ohm (less current but lower max voltage drop)

Do you agree with these measurements/statements?

Best,

C.

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