Chapter 5

RPC upgrades and new RPC detectors

5.1 Overview and Motivations

The Resistive Plate Chamber system (RPC), located in both barrel and endcap regions, provides a fast, independent muon trigger over a large portion of the pseudorapidity range ($|\eta| < 1.6$). It also contributes to muon reconstruction and identification adding redundancy to the muon system in particular regions where geometrical cracks are present in the other muon sub-system.

During High-Luminosity LHC (HL-LHC) operations the expected conditions in terms of background and pile-up will make the identification and correct P_t assignment a challenge for the Muon system. The goal of the RPC system is to provide additional hits with coarse spatial resolution and high time precision to be used at trigger and reconstruction level. The impact of such redundant system will be crucial during phase II of LHC operations to mantain the largest possible number of reconstructed hits also in presence of aging of the present muon detectors.

The RPC Upgrade is based on two projects: an improved Link Board System and the extension of the RPC coverage up to $|\eta| = 2.4$. [FIXME 2.4 or 2.5?]

The Link Board system, that will be described in section 5.2, is responsible to process, synchronize and zero-suppress the signals coming from the RPC front end boards. The Link Board components have been produced between 2006 and 2007 and will be subjected to limitations and failure in the long term as will be described in section 5.3.4. The upgraded Link Board system will overcome the present limitations and will improve the precision in the timing readout allowing to explore the full RPC intrinsic time resolution at the level of 1 ns. At moment indeed signals coming from the RPCs are elaborated by the Link Board system and digitized with a precision of one bunch crossing although the detector itself has an intrinsic time resolution of about 1 ns.

An extension of the RPC system up to $|\eta| = 2.1$ was already planned in the CMS TDR ?? and staged because of budget limitations and expected background rates higher than the rate capability of the CMS RPC technology used for the present system. An extensive R&D program has been done in order to develop an improved RPC that fulfills the new CMS requirements. Two new RPC layers in the innermost ring of stations 3 and 4 will be added to improve the redundancy of the muon system also in the region above $|\eta| = 1.6$ where the higher background is expected and the magnetic field is less uniform.

5.2 The present RPC system

The RPC system is organized in 4 stations called RB1 to RB4 in the barrel region, and RE1 to RE4 in the endcap region. The innermost barrel stations, RB1 and RB2, are instrumented with

2738 ~~2 chambers of RPCs facing the inner (RB1in and RB2in) and outer (RB1out and RB2out) sides~~
2739 ~~of the DT chambers~~. All other RPC stations in the barrel and in the endcaps have one RPC.
2740 Every chamber is then divided from the read-out point of view into 2 or 3 η partitions called
2741 *rolls*. The RPC system consists of 480 barrel chambers and 576 endcap chambers. Details on the
2742 geometry are discussed in the paper ??.

2743 The CMS RPC chamber is a double-gap, operated in avalanche mode to ensure reliable oper-
2744 ation at high rates. Figure 5.1 shows a schematic view of the double gap RPC with strips in
2745 middle.

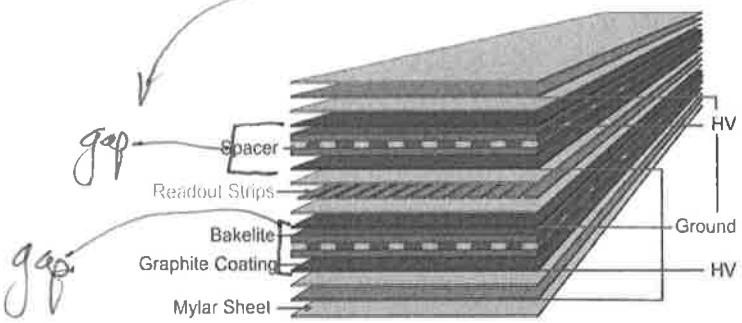

Figure 5.1: Schematic view of the double Gap design of the RPC chambers. Strips are placed in
the middle between the two RPC gas gaps.

2746 Each RPC gap consists of two 2-mm-thick resistive High-Pressure Laminate (HPL) plates sep-
2747 arated by a 2-mm-thick gas gap. The outer surface of the HPL plates is coated with a thin ~~con-~~
2748 ~~ductive~~ graphite layer, and a voltage is applied. The RPCs are operated with a 3-component,
2749 non-flammable gas mixture consisting of 95.2% freon ($C_2H_2F_4$, known as R134a), 4.5% isobu-
2750 tane (i-C_4H_{10}), and 0.3% sulphur hexafluoride (SF_6) with a relative humidity of 40% - 50%.
2751 Readout strips are aligned in η between the 2 gas gaps and have a strip pitch ranging between
2752 2.28 and 4.10 cm in the barrel and between 1.74 and 3.63 cm in the endcap, according to the
2753 ~~stations ??~~. Signals coming from the strips are asynchronously sent to the Front End boards
2754 whose output is a shaped and discriminated LVDS signal.

2755 The discriminated signals coming from the Front End boards feed via twisted cables (10-20 m
2756 long) the Link Board System located in UXC on the balconies around the detector. The Link
2757 System consists of the 1376 Link Boards (LBs) and the 216 Control Boards (CBs), placed in 108
2758 Link Boxes. The Link Box is a custom crate (6U high) with 20 slots (for two CBs and eighteen
2759 LBs). The Link Box contains a custom backplane to which the cables from the chambers are
2760 connected, as well as the cables providing the LBs and CBs power supply and the cables for
2761 the RPC Front End Boards control ~~with use of the~~ I2C protocol (through the CB). The backplane
2762 itself contains only connectors (and no any other electronic devices).

2763 The Link Board has 96 input channels (one channel corresponds to one RPC strip). The input
2764 signals are the ~100ns binary pulses coming from the Front End Boards (FEB) which are syn-
2765 chronous to the RPC hits, but not to the LHC clock (which drives the entire CMS electronics).
2766 Thus the first step of the Link Board system is the synchronization, i.e. assignment of the sig-
2767 nals to the Bunch Crossing (BX: 25ns periods). Then the data are compressed with a simple
2768 zero-suppressing algorithm. The input channels are grouped into 8 bit partitions, only the par-
2769 titions with at least one nonzero bit are selected for each BX. Next, the non-empty partitions
2770 are time-multiplexed i.e. if there is more than one such partition in a given BX, they are sent
2771 one-by-one in consecutive BXes. The data from 3 neighbouring LBs are concentrated by the

middle LB which contains the optical transmitter for sending them to the USC over a fiber at 1.6 Gbps.

The Control Boards provide the communication of the control software with the LBs via the Front-End Controller (FEC)/Communication and Control Units (CCU) system . The CBs are connected into token rings, each ring consists of 12 CBs of one detector tower and a FEC mezzanine board placed on the Clock & Control System (CCS) board located in the VME crate in the USC. In total, there are 18 rings in the entire Link System. The CBs also perform automatic reloading of the LB's firmware which is needed in order to avoid accumulation of the radiation induced SEUs in the LBs firmware.

The High Voltage power system is located in USC, not exposed to radiation and easily accessible for any reparation. A single HV channel powers 2 RPC chambers. The Low Voltage boards are located in UXC on the balconies and provide the voltage to the front end electronics.

5.3 Resistive Plate Chambers Longevity

5.3.1 Expected rates and integrated charge in the present system

The data collected during 2016 CMS operations allowed to study the values of the background rate in the full RPC system. In Figure 5.2, the distribution of the chamber background hit rate per unit area is shown at a luminosity of $5\times10^{34}\text{cm}^{-2}\cdot\text{s}^{-1}$ linearly extrapolating the data collected during 2016 [ref mentioning the linear dependency of rate vs lumi]. The maximum rate per unit area at HL-LHC conditions is expected to be of the order of 200 Hz/cm^2. In araallel, Fluka simulations have been conducted in order to understand the background at HL-LHC conditions. The comparison to the data has shown, in figure 5.3, a discrepancy of a factor 2 even though the order of magnitude is consistent. A conservative approach is to apply a safety margin of 3 to the extrapolated rates and qualify the RPC performance up to a background rate of 600 Hz/cm^2. [Understand mismatch.]

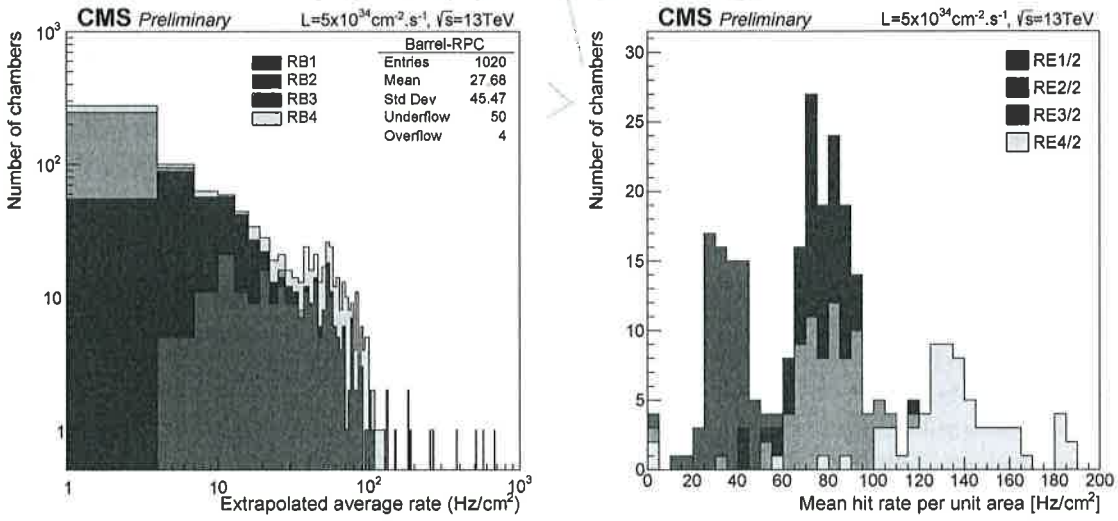

Figure 5.2: (left) Extrapolation from 2016 data of single hit rate per unit area in the barrel region. (right) Extrapolation from 2016 data of single hit rate per unit area in the endcap region.

The total integrated charge expected by the end of HL-LHC, is extrapolated by the currents

5.3.2.2 Alternative options

If suitable eco-friendly gases are not found, the following steps are planned:

- Install a commercial abatement system to *burn off* the RPC exhaust gas. These units are commonly used in the semiconductor industry and several manufacturers are available.
- The previous step will be effective only if all the RPC gas flush through the exhaust where it can be burned off. Currently the RPC system leaks about 1100 liters per hour due to 47 leaking chambers around the barrel system. The plan is to reduce these leaks below 50 l/hour ... plans on how to do
- Add a recuperation system for RPC gases. Once the largest fraction of the gas go through the exhaust it can be easly recovered .... .

5.3.3 Front-end board longevity

The RPC on-detector electronics consists of LV distribution boards, which distribute LV power and slow-control signals, and Front-End Boards (FEBs) which amplify and discriminate the signals induced on the strips and transmit them to the RPC Link Board system located in the CMS tower racks.

During Run-I, very few failures or malfunctioning of FEBs (23 over 6016) have been reported. The FEBs had been previously tested up to a neutron fluence of about 10^{12} n/cm^2 and no damage was observed [41]. In order to qualify the FEBs performance at the higher doses and fluence, a new campaign of neutron irradiation testing is planned. Since the FEB electronics is basically analog, Single Event Upsets (SEUs) would negligibly increase the spurious noise rate. In addition, by the end of Run-I, about 1% of RPC electronic channels were masked due to a failure in the distribution board caused by discharges in the chamber. A new generation of distribution boards, with stronger protection against discharge, has been already produced and 23 out of 360 barrel distribution boards have been replaced during LS1.

5.3.4 Limitations of the RPC Link Board System

[add limitations due to 25 ns] The RPC Link Board (LB) System receives the data from the detector Front End Boards via the copper cables in the LVDS format, then synchronizes them, compresses and sends them via the optical links to trigger processors, the Concentrator Cards in the barrel (*TwinMux*), the Overlap Muon Track Finder (OMTF) in the overlap region and Concentrator and Pre-Processor Fanout (CPPF) in the endcap. Both Link Boards and Control Boards (CB), responsible to control the communications between LBs, are based on the Xilinx Spartan III FPGAs, the CB additionally contains radiation-tolerant (FLASH based) FPGA Actel ProAsicPlus. The Link Board System components were produced between 2006 and 2007. It is a custom electronics containing many different devices. High-Temperature Operating Life (HTOL) has been performed by the Xilinx company in order to estimate the failure rate of the FPGA devices. From these tests, few FPGA chips failures can be expected during 20 years of operation of the RPC link system (it contains in total 2860 Spartan III FPGAs). For other devices used on the LBs and CBs (FLASH memories, TTCrx, GOL, CCU25, QPPL ASICs) such estimations are not available. [to be mentioned the spares sistuation] The ionising radiation levels on the detector balconies is relatively low, therefore it was used on the LBs and CBs the SRAM based FPGAs which are vulnerable for the Single Event Upsets (SEUs). In run 2, to avoid accumulation of the radiation induced SEUs the firmware is reloaded periodically (every 10-30 min). These methods work well; we have not observed any significant impact of the SEU on

the system performance. During the LHC operation the SEU-like problem is detected by the online software with frequency of one error per a few days (for the full system). The CBs are connected into FEC token rings, therefore if one CB fails then the entire ring does not work, leading to a loss of a significant part (1/18) of the system. Moreover, the identification of the malfunctioning board is difficult and time consuming, preventing prompt reparation during any short break of the LHC operation. The CBs are connected into the token rings with copper Ethernet cables, some of them are over 10 m [FIXME] long. Therefore, the ring operation can be disturbed by the electromagnetic noise which results in the errors during the software read or write operations. The impact of this problem was minimise by a modification of the CB hardware and firmware. Additionally, in the control software the methods for auto-recovery after the errors in the ring operation were implemented. As a result, the CCU errors are relatively rare now, however still sometimes results in a problem with the configuration of the Link System for the running. The above problems lead only a few time to a loss of the beam time during the LHC operation between 2010 and 2016. However, it is possible that with the aging of the electronics they may become more frequent.

5.4 Upgrade of the RPC Link Board System

The number of components of the present Link Board system as described in the section 5.2 is reported in table 5.1. In view of an upgrade of the system all the Link Boards, Control Boards, Front planes have to be replaced. The fibers have been certified to work up to 5Gbps depending on the length and the possibility to maintain them in the new upgraded system has to be checked.

Table 5.1: Number of components of the Link Board system

item name	quantity
Link Boards	1376
Control Boards	216
Link Boxes	108
Front planes	216
Optical links	492
12-channels fibers (from CBs to FECs)	18
TTC fibers	216

5.4.1 Motivations for a new Link Board System and use of RPC timing

As reported in section 5.3.4 the present Link Board system could not perform with the same efficiency in the long term. A new system is needed to improve the robustness of the RPC readout and the possibility to upgrade and maintain the firmware. In addition the new LB system will be upgraded in such a way to explore the full timing capabilities of the detector at trigger and reconstruction level.

Although the RPC detectors have an intrinsic time resolution [cite paper] of the order of 1ns, the link board system based DAQ system of the RPCs during phase 1 records the RPC hits informations at steps of one BX (25 ns) loosing the full timing power of the detctor.

The link board upgrade proposed for phase 2 will overcome this limit enhancing the performance of the system from the timing point of view. The higher background expected for the phase 2 LHC operations will be strongly mitigated by the precise timing tag of the RPC with benefits for the RPC sunchronization proecedures and to reject background hits.

During phase 2 the muon trigger system will be reviewed and a possible approach is to analyze all the hits coming from DT, CSC and RPC in a global way in the new back-end of the muon trigger. The information of a precise timing from the RPC hits will be available at trigger level very soon and can be used to reject out-of-time muons and background hits.

Moreover the timing informations coming from the muon system have a key role in the HSCP analysis (see section on physics and trigger: camilo+Luigi). During phase 1 DTs and CSCs timing have been used at offline level together with the RPC information with BX granularity to identify slowly moving stable charged particles. No dedicated trigger using timing informations is available. In phase 2 the fast and precise timing from the RPCs can be available at trigger level and can be used to define a HSCP dedicated trigger implementing a coherent out-of-time coincidence of hits in the RPC stations. Section 8.3.2 [to be checked] describe the RPC based algorithm to trigger HSCP particle in phase 2. Figure 8.14 [to be checked] shows the comparion of the efficiency as a function of β in the case of the L1SingleMuOpen trigger presently used for this analysis (left) and the RPC-based trigger proposed for phase II (right).

5.4.2 The new Link Board System

Based on previous explanations about link board (LB) and control board (CB) limitations, the performance of some components such as CCU and TTCrx chips are not efficient. In addition, CCU, TTCrx GOL and QPLL ASICs are not available now. Since redesign of these ASICs are time consuming and overpriced, so suitable alternatives must be found. One of the best ways to overcome the present limitations is implementation of these chips by FPGAs. Since FPGAs are truly parallel in nature so different processing operations do not have to compete for the same resources and each independent processing task is assigned to a dedicated section of the chip and can function autonomously without any influence from other logic blocks. Therefore for true parallel coincidence execution between the signals from many RPC detectors with the LHC clock, FPGA is the best candidate. In addition, FPGA chips can keep up with future modifications that might be necessary. As a product or system matures, the performance of the link board can be improved without spending time for redesigning hardware or modifying the board layout, which is a grate feature for future upgrades of Muon system. Although, implementation and optimization of four important chips of LB and CB by FPGA is a new challenge, the design, implementation and testing of TTCrx core already done by INFN group for the RE4 development, shows that this approach can be satisfactory, and considering in addition the possibilty to correct for SEUs, that was not included in the previews implementation.

5.4.2.1 Radiation effects on commercial FPGAs

Most Commercial chips can be safely used for Total Ionization Dose (TID) of few krad. Since the TID on place of LB for 10 years work of LHC with nominal luminosity, is below 100 rad, the TID is not a problem and there is no need to use radiation hardened electronics. Therefore, the GOL chip and other radiation hardened chips which can be safely used even for TID in order of Mrad are overqualified for the LB system. But the most important radiation effects i.e., SEU on RAM-based or FLASH based commercial FPGAs must be corrected. The experimental results on the FPGA-GTX show that the SEUs only cause rare transient bit errors in the data and no mitigation is needed. But, for Configurable Logic Block (CLB) and Block RAM (BRAM) of new family of FPGAs, the effect of SEU is more complicated.

In new FPGA families, the transistor size has dramatically decreased, enabling more configuration logic cells to be packed into the same amount of physical area due to the smaller process technology of each family. The amount of area affected by one radiation particle strike has not changed, but the number of logic cells and transistors inside that area has increased. In ad-

dition, the smaller transistors have lower threshold which make it easier for the logical value stored in the SRAM cell to experience an upset. So, performing the error correction techniques on one of important building blocks of new FPGA families i.e., CLB is more critical. The SEU typically affect a single bit in a single cell of FPGA BRAM, which can be mitigated by error detection and correction methods. The calculations based on experimental results show that without considering the chip cores which are implemented by FPGA, by using Vertex 6 instead of Spartan III in LB and CB, the SEU in CLB will be around five times greater. So, GOL, CCU, QPLL and TTCrx cores must be implemented by suitable commercial FPGAs through some reliable SEU mitigation capabilities in comparison to present LB system.

5.4.2.2 SEU Mitigation in FPGA

Since all the ASIC chips of the LB and CB must be implemented by FPGA, applying suitable SEU mitigation methods for different FPGA areas are more critical. All SRAM or FLASH based FPGAs, contain SRAM blocks and flip-flops (FF) which are susceptible to SEUs. The SRAM cells have a very high susceptibility to SEUs. So, the FPGAs using SRAM cells for device configuration will need special mitigation techniques in order to prevent loss of functionality when struck by a heavy ion. The FFs which are the most robust of memory structures are only upset in high-radiation environments. There are several methods for SEU correction such as Error Correction Code (ECC), Cyclic Redundancy Check (CRC), Blind Scrubbing, Read back Scrubbing, Configuration Scrubbing (CS), Memory Scrubbing and Triple Module Redundancy (TMR). If the upset occurs in data SRAM, error detection and correction (EDAC) techniques can be used to mitigate the error. The ECC is a redundancy coding mechanism that is useful for correcting Single Bit Upsets (SBU). CRC is particularly useful for detecting Multi Bit Upsets (MBU) across an FPGA. Although, any multi-bit error requires the device reconfiguration, but since in the new families of Microsemi FPGAs, SRAM bits in each logical word are physically separated, the probability of the MBU resulting in uncorrectable errors is dramatically reduced. The built-in ECC feature in FPGAs can be used to protect data integrity and prevents software controlled write and read process for BRAM memory tests. The experimental results for FPGA Vertex 6 show that even by using the simple ECC method, the SEU Mitigation strategy completely works and no errors are detected in the BRAM contents.

If the error occurs in the SRAM configuration memory used to control the *personality* of an SRAM-based FPGA, a logic failure or firm error of the FPGA may result. In this case, the simple blind scrubbing strategy which is used in current LB, continuously overwrite to the configuration memory from a protected golden file. Although, this method has fast correction speeds, but inherently is unable to detect upsets. Moreover, inefficiently a significant portion of processing bandwidth is wasted continuously for reconfiguration of unaffected FPGA's configuration memory. This problem can be solved by Flash-based FPGAs or CS technique in SRAM-based FPGAs. In CS method, the memory is checked periodically, the upsets are detected and the dynamic partial reconfiguration is used to overwrite the upsets. The initial configuration must first be completed before any scrubbing can occur. The CS method is usually performed at periodic intervals while the FPGA is in operation (dynamic reconfiguration). This partial reconfiguration is not intended to interrupt normal FPGA operation.

The TMR in SRAM-based FPGAs are used for SEU in logic and FFs and for the Flash-based FPGAs it is only used for SEU correction in FFs. In a design with TMR method, the design circuitry is triplicated into three identical copies and typically placed at three different locations in the FPGA. Such solution provides protection against SEU in the registers, however it does

station. GE2/1 is part of the present tdr for the station 2, and RE3/1 and RE4/1 are described here with the goal to add the redundancy in the last two endcap stations.

The RPC upgrade is essentially driven by the necessity to increase the numbers of muon hits up to —η—=2.4 and to provide also timing informations at level of 1 ns.

CSC system provide high efficiency for identification and triggering of muons in the endcap region. Nevertheless as can be seen in figure 5.11 there are gaps between CSC chambers where the identification and the trigger performance are lower because of the reduced number of segments available. Even for a perfectly working system there are dips in the CSC efficiency due to the high-voltage spacers inside the CSC chambers.

Hits coming from RPC stations add the needed redundancy in such regions providing appropriate spatial resolution to correctly contribute to the P_t assignment. Impact of RPC hits on the single muon trigger efficiency can be seen on figure 5.11. [this figure is in preparation and should replace the one at moment present].

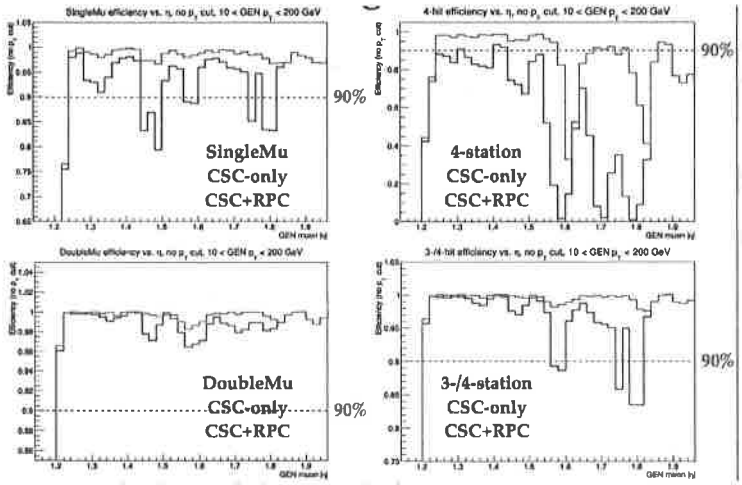

Figure 5.11: Impact of RE3/1 and RE4/1 hits inclusion on the single muon trigger efficiency.

RPC informations will be also useful to remove the CSC ambiguity in cases where two or more segments are reconstructed in the same CSC chamber. Extrapolating the experience from the present operations up to the HL-LHC luminosity, the chance to have a fake Local Charged Tracks (LCTs) inside one ME3/1 or ME4/1 chamber, is 13%. These extra LCTs when reconstructed in presence of a real muon can result in a hight p_T muon solution in the Endcap Muon Track Finder, even though the actual muon has low p_T.

The plan for the RE3/1 and RE4/1 envisage a 2D strip readout measuring the arrival time of the RPC signal on both ends of the strip and recovering the position along the strip looking at the time difference [see section elctronics and layout]. With such method a resolution of the order of few cm is expected so that the CSC ambiguity can be removed directly at station level.

The advantages already described in having an improved timing of the RPC system will be extended to this region with the RE3/1 and RE4/1 installation.

In HSCP searches between 11 and 14 % of the events are in the region covered by the RPC extension (figure 5.12). A dedicated HSCP trigger based on RPC hits will extend the discovery reach in this region [ref camilo section].

5.5.2 Overview of the requirements and technological choices

The two new stations of RPCs, RE3/1 and RE4/1, will be installed in muon disks 3 and 4 respectively, covering the $1.8 < |\eta| < 2.4$ region and complementing the already existing CSCs in that range in stations ME3/1 and ME4/1. [make reference to a picture]

RE3/1 will be located in the radial range R=1526÷3302 mm, while RE4/1 in the range R=1709÷3290 mm. A schematic view of the chamber dimensions is shown in figure 5.13. [check numbers and improve picture]

According to FLUKA simulations and by a comparison with CSC chambers already located

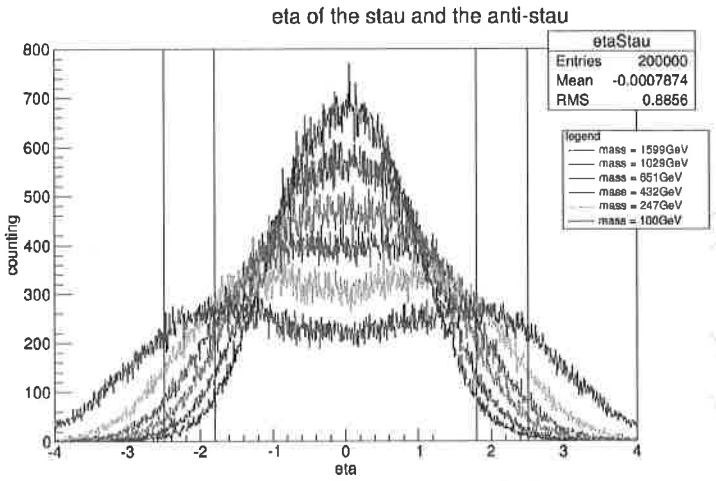

Figure 5.12: Eta distribution of the HSCP particles for different masses. The lines at η=1.8 and 2.4 define the region covered by RE3/1 and RE4/1.

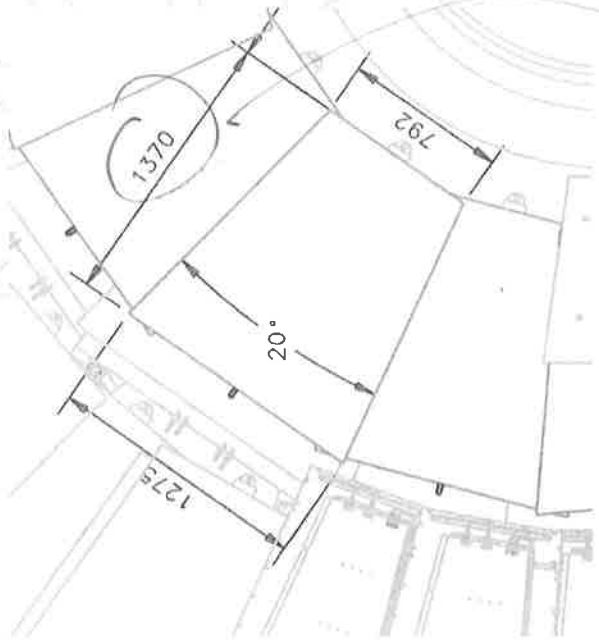

Figure 5.13: Detector envelope for the RE4/1 chambers.

in the region where RE3/1 and RE4/1 chambers will be mounted, a rate of about 2kHz/cm^2 (including a safety factor of 3) is expected in the hottest points of these new RPC stations (figure 5.14).

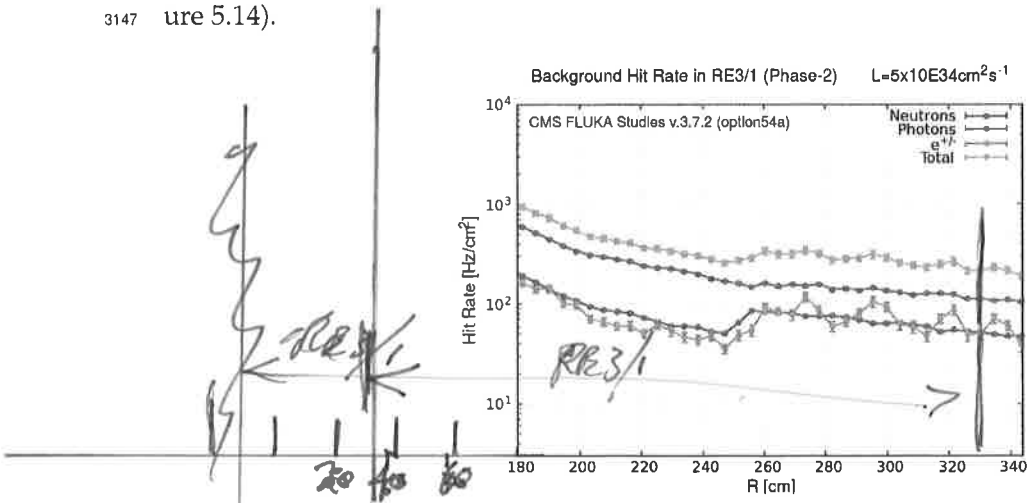

Figure 5.14: Expected rate for HLC Luminosity of 5×10^{34} cm^{-2}s^{-1} in the region covered by the RE3/1.

To sustain the expected rates and perform with efficiency above 90% also in this region an improved version of the RPCs (*i*RPCs) has been developed.

The rate capability can be imporved in various ways:

- Reducing the elctrode resistivity and/or thickness, wich has the effect of reducing the recovery time needed for the electrodes to be charged up again after a discharge in the gas gap.
- Reducing the average charge generated in the avalanches, and transferring part of the signal amplification from the gas to the front-end electronics. Reducing the overall charge path in the gap indeed results in a reduced voltage drop on the electrode plates, and a reduced period of inefficiency; this also reduces the aging process.
- Changing the detector configuration, which includes different number of gaps, different gas and electrode thickness, that could enhance the performance of the detector.

In addition, aging effects during the full HL-LHC program need to be accurately considered, as discussed in the section 5.x.x for existing detectors. For an expected rate of 2 kHz/cm^{-2} and an average charge per avalanche of 20 pC, the integrated charge in the detector after the integrated luminosity of 3000 fb^{-1} will reach about 2 C/cm^2 (including always a safety factor of 3). Tests at GIF++ have been planned in order to integrate the full charge during the second part of 2017 and 2018.

The more natural technological choice is to implement small modifications to the detector layout of the present RPC system in order to fulfill the HL-LHC requirements. The starting point is the double gap with electrodes done of High Pressurized Laminated (HPL) commonly known as bachelite. Working prototypes have been also produced with low resistivity glass (10^{10} $\Omega\cdot$ cm) [reference to GRPC] that due to its stiffness can be realized with plates as thin as 0.7 mm. Although glass electrodes are very attractive with the possibility of having very thin gaps and thus a reduced avalanche charge, the limited size of this kind of glass (30 · 32 cm^2) does not allow the realization of large RPC detector in a simple way, so this material will be considered

only as backup solution for the HPL baseline option.

From the readout point of view as reported in the section [rpc upgrade motivations] we need to provide RPC hits with a time resolution of the order of 1 ns and a spatial resolution of the order of few mm in the phi direction. In addition a resolution of few cm in the η direction will help to remove CSCs ambiguities when more muons cross the same chamber.

5.5.3 Baseline option: Double gap RPCs

To satisfy the requirements mentioned in the previous section, as baseline option, we adopt a detector working in lower-gain avalanche-mode operation to achieve a higher rate capability of far exceeding 2 kHz cm^{-2} as well as to ensure the longevity of the RPC gaps[42].

As in the case of the present system a double gap readout with pick-up strips in the middle is considered.

To reduce the detector aging and to improve the rate capability both the electrode and gas gap thickness are reduced and part of the amplification is moved to an improved front-end electronic [ref. electronic chapter].

Improving sensitivity of pulse-digitization electronics is the major factor to enhance both detector rate capability and longevity for the CMS RPCs. In addition reducing the electrode thickness and keeping its resistivity in the range $0.9 \div 3.0 \times 10^{10}$ ohm cm reduce the recovery time of the electrodes and imporve the rate capability as well.

In the present baseline design for the *i*RPCs, a thickness of 1.4 mm for both gaps and electrodes is chosen instead of the 2 mm used for the current CMS double-gap RPCs.

We systematically examined the pickup charges of the avalanche pulses drawn in six double-gap RPCs constructed with gap thicknesses ranging between 1.0 and 2.0 mm [?]. Figure 5.15 shows the pickup charges drawn in the 1.2- (squares), 1.4- (triangles), 1.6- (open circles), and 2.0-mm (full circles) double-gap RPCs as a function of the electric-field intensities whose values were converted to the effective ones under the standard conditions of P = 1013 hPa and T = 293 K. The tetrafluoroethane-based gas mixture for the standard CMS RPC operation (95.2% $C_2H_2F_4$, 4.5% i-C_4H_{10}, and 0.3% SF_6) was used for the data.

Figure 5.15 clearly shows that the thinner gap thicknesses more effectively retard the fast growth of the pickup charges of the ionization avalanches even in the low electric field regions. This implies that the use of the thinner gaps will effectively preserve the size of the operational plateau when we lower the digitization threshold to enhance the detection sensitivity. The reduction of the operational high voltage as the result of decreased gap thickness and of the digitization threshold will also imporve the robustness of the system preventing high voltage failures and improving the safety of the detectors.

A gas gap and electrode thickness of 1.4 mm is chosen as baseline solution to be more safe during detector production. Thinner gas gaps will be more sensible to any disuniformity in the distance between electrodes so that 1.4 mm is considered a safe compromise for CMS application.

The electrode resistivity is maintained in the range from 0.9 to 3.0×10^{10} Ω cm and can be achieved with high pressurized larminated (HPL, Bakelite) as for the present RPC CMS system. Resistivity values lower than the range explored make the detector behaviour unstable and have not been considered for the RPC upgrade program.

The pick-up strips are placed in the middle between the two RPC gaps and are embedded

in a readout board made of two parts; a large trapezoidal Printed Circuit Board (PCB) and a mezzanine. The PCB hosts 192 strips with a pitch of 6 mm at the lowest eta position of the chamber, up to about 3.75 mm at the highest one. More details are reported in section 5.5.6.2.

5.5.3.1 RPCs Performance tests and aging studies

In order to validate the peformance of the thinner double-gap RPC baseline option, smaller size prototypes have been tested at KODEL with cosmic rays in presence and without gamma irradiation. Large size chambers have been tested in dedicated test beam at GIF++.

In KODEL a prototype of 1.4-mm double-gap RPC was examined with cosmic muons using a voltage sensitive front end board with a threshold value of 300 μV. This value corresponds to a threshold of about 50 fC in the charge; about a factor 3 lower than the value of the present RPC system Front-end electronics.

Figure 5.16 shows the detection efficiency (ε_μ) and the cluster size ($< C_s >$: number fired strips per hit) (left plot) and ε_μ and the probability to have cluster size above 6 strips ($P(C_s > 6)$) (right plot) as a function of the effective Voltage (HV_{eff}[43]) measured under a condition of no gamma background. The working voltage HV_{WP} for the 1.4-mm double-gap RPC is defined as the voltage at which the efficiency reaches 95% + 110 V.

A criterion of evaluation for the rate capability of the trigger RPCs will be rather realistic when defined as a background rate at which the shift of the WP approaches the size of the operational plateau. The detector properties related with the high-rate background were crucially examined using a 5.55-GBq ^{137}Cs source.

In Fig. 5.17, ε_μ and $< C_s >$ (left plot) and ε_μ and $P(C_s > 6)$ (right plot) are shown for the 1.4-mm double-gap RPC at a fixed threshold value of 300 μV and with three difference gamma fluxes. The strength of the gamma flux impinging in the RPC was adjusted by the distance of the detector from the gamma source (triangles and squares measured at 38 and 28 cm, respectively) and by using a lead absorber (full circles measured with an absorption factor of about 2.5 by using a lead observer at 38 cm). The rates, R_{clus} (rate of clusters) and R_{str} (rate of strips), measured at the working point with the largest gamma flux yields at 28 cm were 1.85 and 4.14

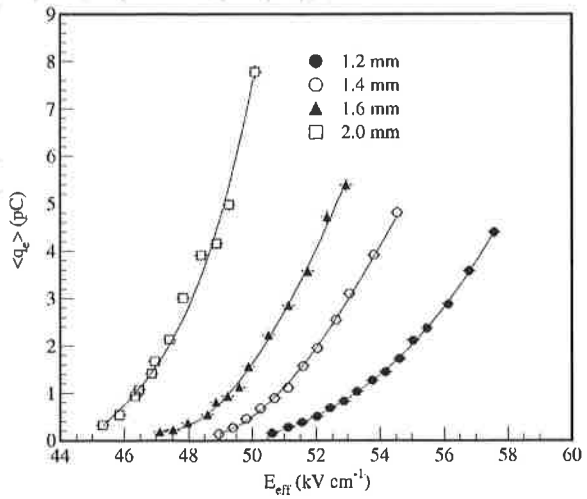

Figure 5.15: Mean fast charges measured on 1.2- (full circles), 1.4- (open circles), 1.6- (triangles), and 2.0-mm (squares) double-gap RPCs, as a function of the electric field intensity.

kHz cm^{-2} respectively. The shifts of the WP obtained from the data labelled with no=gamma (open circles) to the one from the data obtained with the largest gamma flux (squares) was evaluated as 300 V (4% in $\Delta V/V$).

The impact of the gamma background on the efficiency at Working Voltage is shown in figures 5.18. The reductions of the efficiency at the rates of R_{clus} = 1.85 kHz cm^{-2} and R_{str} = 4.14 kHz cm^{-2} was measured as 2.92%.

The previous results show that the impact of the maximum background rate on the RPC performance is negligible on the detection efficiency (less than 3%) while move the working voltage by about 4%. As this voltage shift is lower than the avalanche to streamer voltage separation we do not expect deteriorations of the chamber performance. It should be noted that an authomatic feedback control, tuning online the working voltage as a function of the measured background rate, could be implemented making more stable the detector operations. The residual difference in rate among different points of the same chamber will correspond to working voltage differences lower than 100 volts.

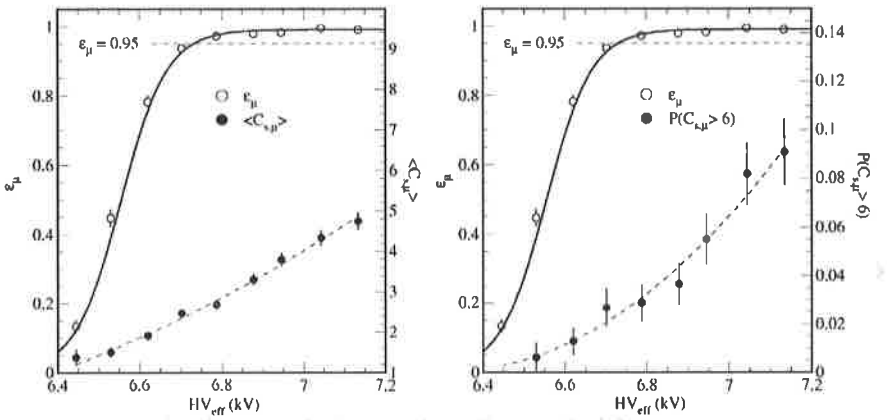

Figure 5.16: ε_μ and $< C_s >$ (left) and ε_μ and P(C_s >6) (right) at Th = 300 μV as a function HV$_{eff}$ measured on the 1.4-mm double-gap RPC under a condition of no gamma background.

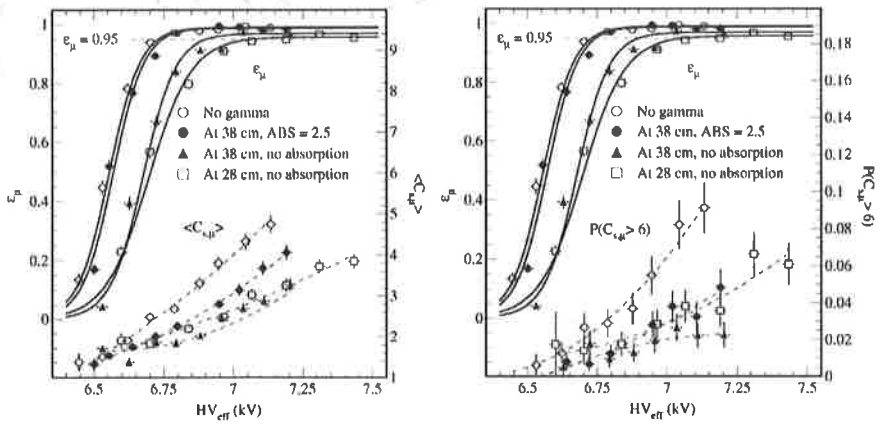

Figure 5.17: ε_μ and $< C_s >$ examined for the 1.4-mm double-gap RPC with a fixed threshold value of 300 μV and with three difference gamma fluxes. The details for the data symbols are described in the text.

All the previous results have been carried on with the current tetrafluoroethane-based gas mixture for the CMS RPC operation (95.2% $C_2H_2F_4$ + 4.5% iC_4H_{10} + 0.3% SF_6).

[add new tests in progress with ecological gas mixture]

The baseline option has already been tested at GIF++ with a full size prototype in a dedicated test beam [describe layout of full size prototype and results]

5.5.4 Technological aspects of bachelite detector production and quality control

In order to maintain stable and reliable detector operations, the mechanical uniformity and the electrical stability of the gas gaps have to be garanteed during the production phase. In addition, the maintenance of initial detector characteristics for the long term CMS operation was also an important factor to be considered for the preparation of the detector production facilities.

The main production chain is almost standard and has been already succesfully implemented [44] during the production of the RE4 chambers at KODEL laboratory. The same production technologies and facilities will be used for the new RPC chambers (RE3/1 and RE4/1).

HPL panels are produced, cutted and cleaned by Puricelli firm in Italy and then delivered to KODEL. Thin graphite layers on both the high voltage and ground side of the gaps are coated by a silk screen method. Both sides are then electrically protected by a 190 μm thick polyester (PET) sheet. Figure 5.19 shows the table used for both operations. Flat metric table is used to glue circular spacers and peripheral edges on the electrod surface in order to maintain the proper gas gap thickness. The finally sealed gap is then oiled to garantee the smoothnes of the surface. Figure 5.20 shows the different facilities used for these operations.

The assembled gaps are tested for mechanical gas tightness test and test of failure of the spacers and for electrical qualification and then sent to CERN for chamber construction and per-

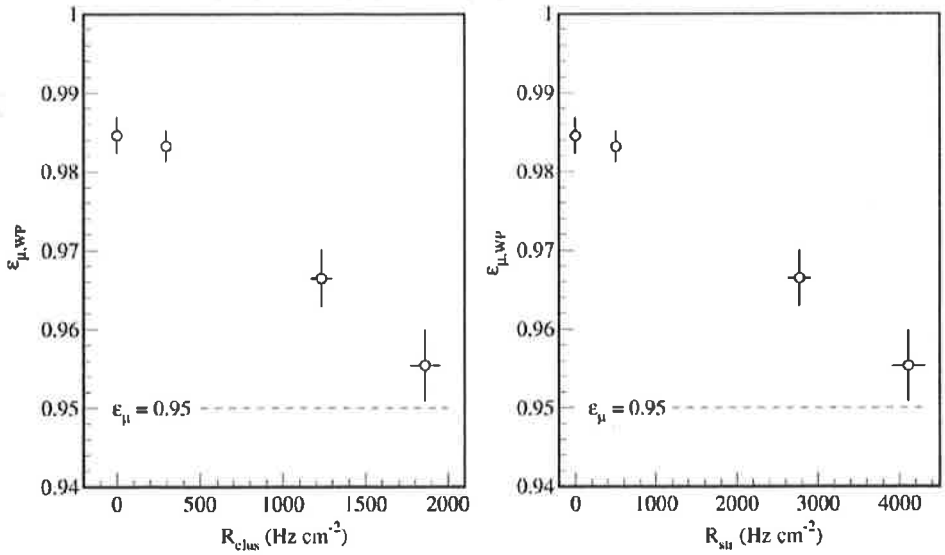

Figure 5.18: WP efficiencies at a maximum rate of $R_{clus} = 1.86$ kHz cm^{-2} (left) or of $R_{str} = 4.14$ kHz cm^{-2} (right) measured for the 1.4-mm double- gap RPC. The data were measured at the fixed threshold of Th = 300 μV.

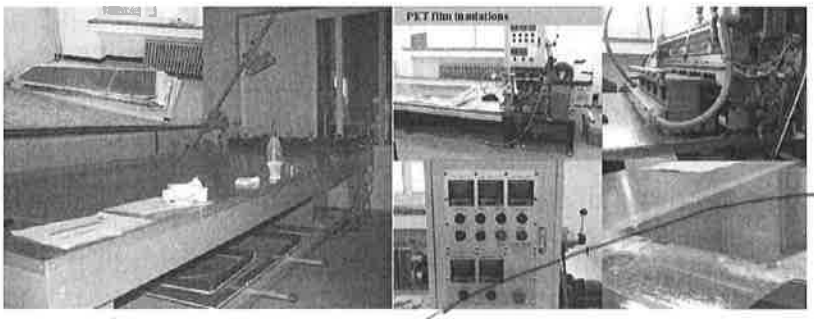

Figure 5.19: Flat metric tables, rubber chambers for pressurization, specially machined jigs to fix the spacers and the peripheries to assemble the gas gaps (left) and oil coating facility composed of two oil tanks, one lifting device, two air pumps, one air compressor, and a press device (right).

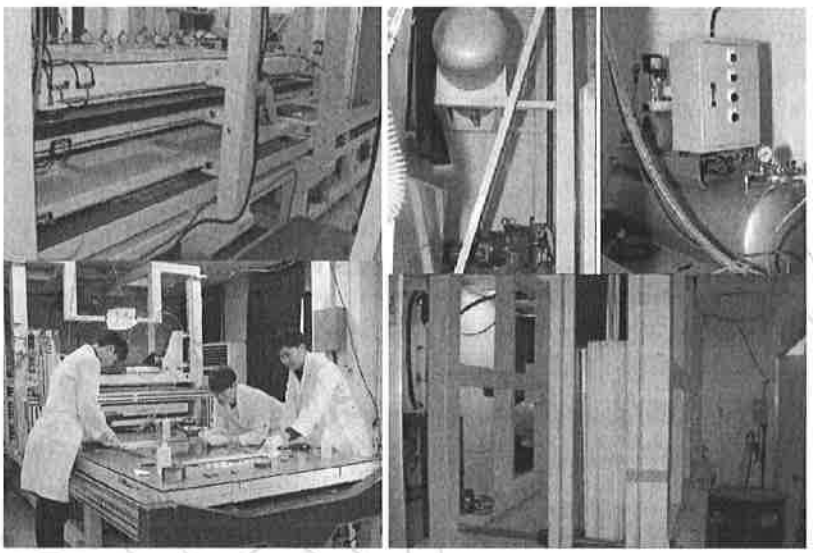

Figure 5.20: Test facility for the mechanical qualification composed of a metric table and a gantry arm equipped with a pencil-shape probe (left) and a pressure chart of testing the spacer failure and the gas tightness (right).

formance tests [45]. Also in this case all the steps of quality control have been succesfully tested during the RE4 production and will be repeated for these new chambers.

5.5.5 Multigap RPC option

As described in the section xxx the RPC time information could improve the background rejection in the high eta region and would improve the search capabilities for HSCP analysis. With a time resolution of the order of 100 ps the improvement are also large. A time resolution of the order of 100 ps can only be reached with the use of multi-gap RPCs. These detectors are built with a number of very thin electrodes separated by short distances of the order of a few hundred microns thanks to the use of fishing lines. As for the single-gap RPC, high voltage is applied only on the external electrodes while the internal electrodes are kept floating. The structure of the mutligap RPC allows the filtering out of the slow avalanche component keeping only the fast one. Consequently an excellent time resolution is obtained with a reduced avalanche charge. Thanks to this, multigap RPC was successfully used as time-of-flight dete

tors in ALICE and STAR experiments. Greater is the number of gas gaps, more effective will be the filtering and thus better will be the timing performance. A time resolution better than 100 ps could be obtained with 6 gaps. To achieve such a performance while using the same electronic readout system proposed for the HPL double-gap baseline scenario, 2×3-gap RPCs are considered as option alternative to the baseline.

Multigap RPCs have been developed up to now using glass electrodes thanks to their exceellent flatness. The flatness and the stiffness are important features that thin plates of other materials such as HPL could not provide. A new kind of doped glass with excellent surface flatness and featuring an ohmic electric resistivity of 10^{10} Ω· cm which is two to three orders of magnitude lower than the float glass was developed by the RPC group of Tsinghua University . The new glass was used to build high-rate multigap RPCs that were successfully tested. These detectors were then adopted as the baseline for the inner Time -Of-Flight detector of the future CBM project in which a flux of several kHz/cm^2 is expected.

The new glass seems to fulfill all the requirements needed to build MRPC for CMS except one feature which is the size limitation of the glass plate. Due to its specific fabrication process involving cutting and polishing slices, only thin plates with a surface not larger than 32 cm × 30 cm could be produced.

To overcome the glass plate limitation and build large MRPC, two methods were developed. The first one uses a special glue (radiation hard) to assemble small plates into one of the desired dimension and then build 5-gaps in the standard CMS way. A detector of 25 cm × 47 cm was built and tested at GIF++ using a customized electronic readout system. Although excellent efficiency was obtained the observed noise rate of 7 Hz/cm^2 and the observation of sparks close to the glues zones led to abandon this method in favor of the other one.

The second method proposes to build a large multigap detector by assembling the small glass plates thanks to a mechanical fixation. In this method fishing lines are used to separate the different pieces and to maintain the gas gap distance as can be seen in Figure 5.21. The detector is placed into a cassette that encloses the PCB and ensures the gas tightness.

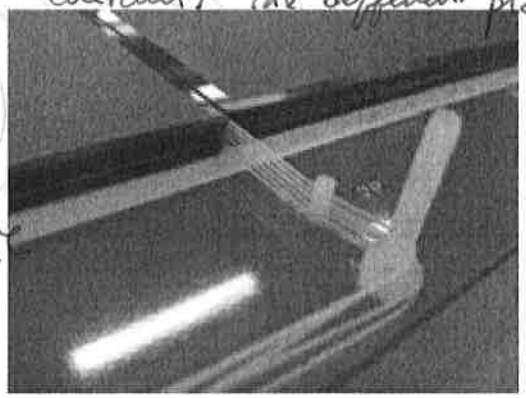

Figure 5.21: A picture of the mechanically assembled multigap RPC detector.

5.5.5.1 MRPC performance in beam test

A 5-gap detector of 25 cm × 47 cm with a 250 µm of gas gap between two consecutive plates was built using the mechanically assembling. The detector was intensively tested at the elec-

tron accelerator ELBE at HZDR using 32 MeV single-electron beam pulses. The flux of the primary beam is tunable from few electrons/s to 107 electrons/s.

Three-component, non-flammable gas mixture composed of 90% $C_2H_2F_4$, 5% C_4H_{10} (isobutene) and 5% SF_6 was used during the test. The gas volume is purged by the flow of the gas mixture with flow rate of 50 ml per minute.

A differential readout system using the NINO chip was used to read out the 12 strips of the multigap RPC and symmetrical and charged opposite HV was applied to the two external plates of the detector. Three TDCs of a CAEN V1290 device were used in the DAQ. The multigap RPC signal leading edge and trailing edge of multigap RPC signals were recorded by two different TDCs. Since there is no external clock signal, RF signal was split and transmitted to the TDCs as a reference for synchronization.

To estimate the multigap RPC time resolution the time difference of the the leading multigap RPC signal and the RF signal time is measured. The Time Over Threshold correction (using the leading and the trailing signal edge time arrival) was used to correct for the time walk. The multigap RPC was then exposed to different particle fluxes to study its efficiency and timing performance. Figure 5.22 shows clearly that this detector could perform extremely well in terms of both efficiency and time resolution up to fluxes of 40 kHz/cm^2.

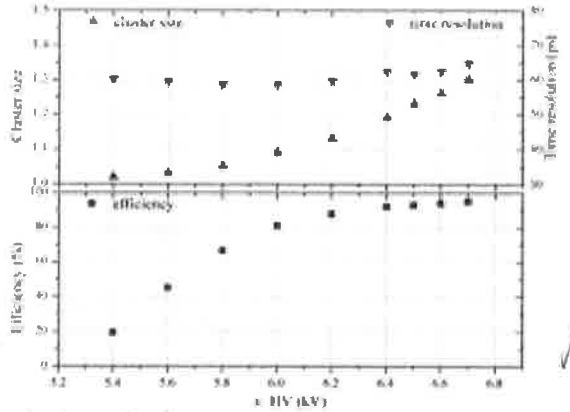

Figure 5.22: Efficiency and time resolution versus the applied HV.

5.5.6 Front-end electronics and DAQ for new detectors

5.5.6.1 Requirements

The new RPC chambers are conceived so that the amount of the avalanche charge associated to the passage of charged particles is reduced with respect to the present CMS RPC. In order to keep the same performance of the latter a new readout system equipped with low noise Front-End electronics able to detect lower charges without affecting detector performance is required.

The Front-End electronics need also to be fast and reliable to sustain the high irradiation environment that will prevail in RE3/1 and RE4/1 in the HL-LHC phase. The new available technologies that allow to minimize the chip size are ideal to be used.

In addition, RPC detectors have fast timing capability. To exploit this feature to improve muon

trigger and physics performance, but also to better localize the η position of the hit, it is important that the new Front-End electronics preserves the RPC signal quality and measures precisely its arrival time.

5.5.6.2 Electronic readout

Several ASICs with low-level noise able to read out the RPC detectors are available. One of these ASICs is named PETIROC (figure 5.23). It is a 32-channel ASIC using a broad band SiGe fast amplifier and a fast SiGe discriminator. Its overall bandwidth is 1 GHz with a gain of 25. Each channel provides a charge measurement and a trigger output that can be used to measure the signal arrival time. It was originally developed by the OMEGA group to read out SiPM devices but its dynamic range (100 fC-400 pC) qualifies it for the readout of RPC detectors as well. Thanks to its low-jitter preamplifier the ASIC jitter is very small and goes below 20 ps for charges above 1 pC in the absence of internal clocks as can be shown in figure 5.24. To uniformise the 32 channels response the ASIC has two adjustment systems. A common 10-bit DAC ensures the trigger level adjustment in the dynamic range. An individual 6-bit DAC is used in each channel to achieve similar response of the ASIC's channels. Figure 5.25 shows the pedestals dispersion before (red line) and after(green line) the adjustment.

Although this ASIC was not developed for CMS, a new version, called CMS RPCROC and taking into account the CMS specifications, is under development. In the new version the charge measurement will be dropped to simplify the ASIC and reduce its cost and power consumption. The charge is roughly estimated using the TimeOverThreshold technique since the PETIROC ASIC allows the time measurements on both rising and falling edges. The lower value of the ASIC dynamic range is also decreased to allow triggering on signals down to 10 fC. The ongoing development on the Front End electronics is common to the one being conducted by the same group to transform the SKYROC ASIC of CALICE into the CMS HGCAL ASIC and will hence benefit from the big efforts made by the CMS collaboration to achieve this[1]. Although the irradiation rate in the RE31 and RE41 is much smaller than the one to prevail in the HGCAL region, the radiation hardness of the new RPCROC ASIC should also get benefit of the HGCAL ROC development in this field. As for the HGCAL ASIC the 350 nm SiGe technology used in the present PETIROC is indeed replaced by the Taiwan Semiconductor Manifacturing Company (TSMC) 130 nm one to increase its hardness. The number of channels is increased from 32 to 64.

To read out the RPC detectors a ~~new readout board is used~~. The board ~~is made~~ of two parts; a large trapezoidal Printed Circuit Board (PCB) and a mezzanine. The PCB, to be inserted between the two RPC gaps in a similar way to the current CMS system, will host 192 strips with a pitch of 6 mm at the lowest eta position of the chamber to about 3.75 mm at the highest one. The strips are separated from the anode of each of the two gaps thanks to a dielectric layer. The thickness of the dielectric layer, its relative permittivity will determine the final impedance of the strips using the HV ground planes placed on the detectors anodes as a reference. Both ends of each strip are connected to two different channels of the RPCROC ASIC.

The ASICs as well as an FPGA device running the TDCs are hosted on the mezzanine that is fixed on the RPC detector ~~cassette~~ (fig: 5.26). To connect a strips end to an ASIC channel a coaxial cable with the same strip impedance is used. It is soldered on one ~~side~~ to the strips end and on the other ~~side~~ to a termination board to be plugged on the mezzanine. This board hosts for each of the connected cable a dedicated circuit to match the ASIC input entry of about

[1]The dynamic range of the CMS HGCAL ASIC is not very well adequate for low charge signal otherwise one can envisage to use it to read out the CMS RPC detectors.

200 Ω. In addition to the 6× 64 channels RPCROCs, the mezzanine has the same number of TDC channels (384). The TDCs will run either on an FPGA or on a dedicated chip. On the same mezzanine an LpGBT chip is ensuring the communication between the RPCROCs and the TDCs on the one hand and a dedicated back-end RPC DAQ board on the other hand. The two boards are connected by an optical link. Thanks to the TDC time precision of the order of 50-100 ps the information of signal time arrival from the strip's two ends will provide the hit coordinate along the strip length with a precision of the order of a few centimeters. This scheme intends to reduce the number of electronic channels by reducing the number of segmentation in η (3 if the readout system of the present endcap chambers is applied) while providing a better spatial resolution.

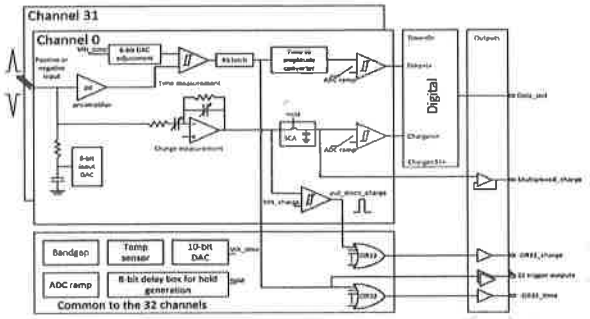

Figure 5.23: The PETIROC schematics.

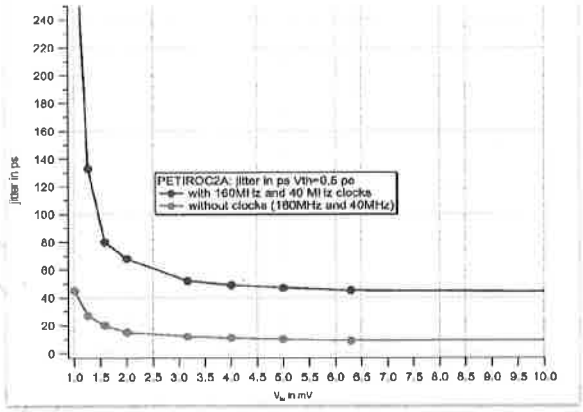

Figure 5.24: The PETIROC time jitter measured with and without internal clocks.

A small board hosting 32 strips, 50 cm long and 4 mm pitch utilizing the before mentioned readout scheme was designed as a demonstrator and then realized (figure 5.27 right). The demonstrator hosts two 32-channel PETIROC ASICs as well as two TDCs implemented on a FPGA. The TDC, developed by the Tsinghua University, uses delay-path based techniques. The TDC was adapted to have 32 independent channels that receive each the trigger output of one of the 32 PETIROC channels. The same FPGA used to host the TDC is used to configure the ASICs thanks to a dedicated firmware providing also the needed state machines that enable recorded data to be properly ordered in time. First tests on the demonstrator have shown that a timing as good as 30-35 ps can be achieved (Figure 5.28) by measuring the difference of time arrival of the signal by two of the TDC channels associated to the two ends of the same strip after an injection of a 10 pC on test points placed on the path of each of the strips. We get 100 ps resolution when 2 pC of charge are injected.

To get the same response of the different ASIC channels to the same injected charge, the individual threshold of each of the channels was fixed in such a way that their pedestals have similar values. This results in similar S-Curves which represent the efficiency as a function of the threshold for a given injected charge (Figure 5.29).

A system allowing the synchronization of the different TDC channels was also developed and implemented as well as an external trigger system. The Active Sensor Unit (ASU) was used to read out one of the current CMS RPC gap (2 mm gas gap enclosed between two HPL plates of 2 mm thickness) on a test bench (Figure 5.30, left) equipped with three Scintillator-PM devices

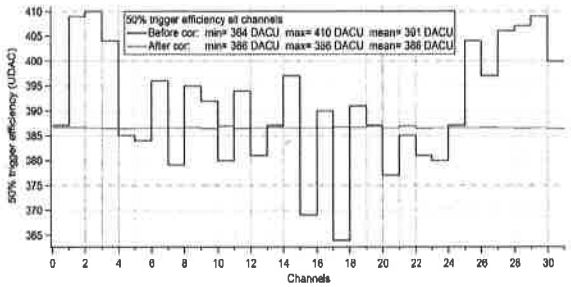

Figure 5.25: Values of the pedestals 50% trigger efficiency of the 32 channels before (red line) the 6-bit DAQ correction and after (green line).

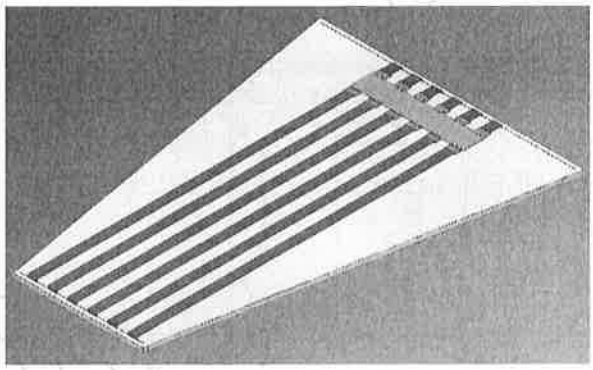

Figure 5.26: Scheme of the new readout electronics. The mezzanine is in green and the coaxial cables coming from the two ends of the strips (violet and red flat cables) are connected to the mezzanine through a matching small orange cards. The detector and the strips-PCB are inside the cassette and are not visible here.

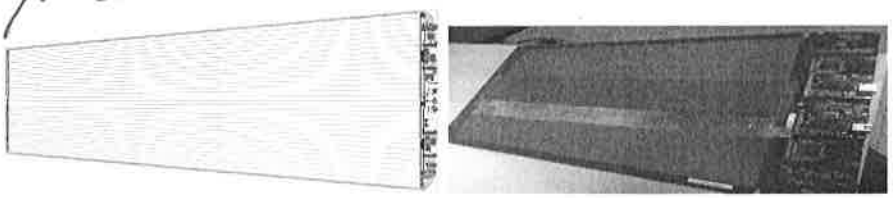

Figure 5.27: Left: Schematics of a large Active Sensor Unit (ASU) with pickup strips read out from both ends by two independent channels of the the same PETIROC. ASICs and TDC on FPGA mezzanines are placed on the outer radius. Right: a picture of a realized small size ASU following the same schematics with pickup strips in the middle.