iRPC front-end electronic status

First prototypes design & test beam results

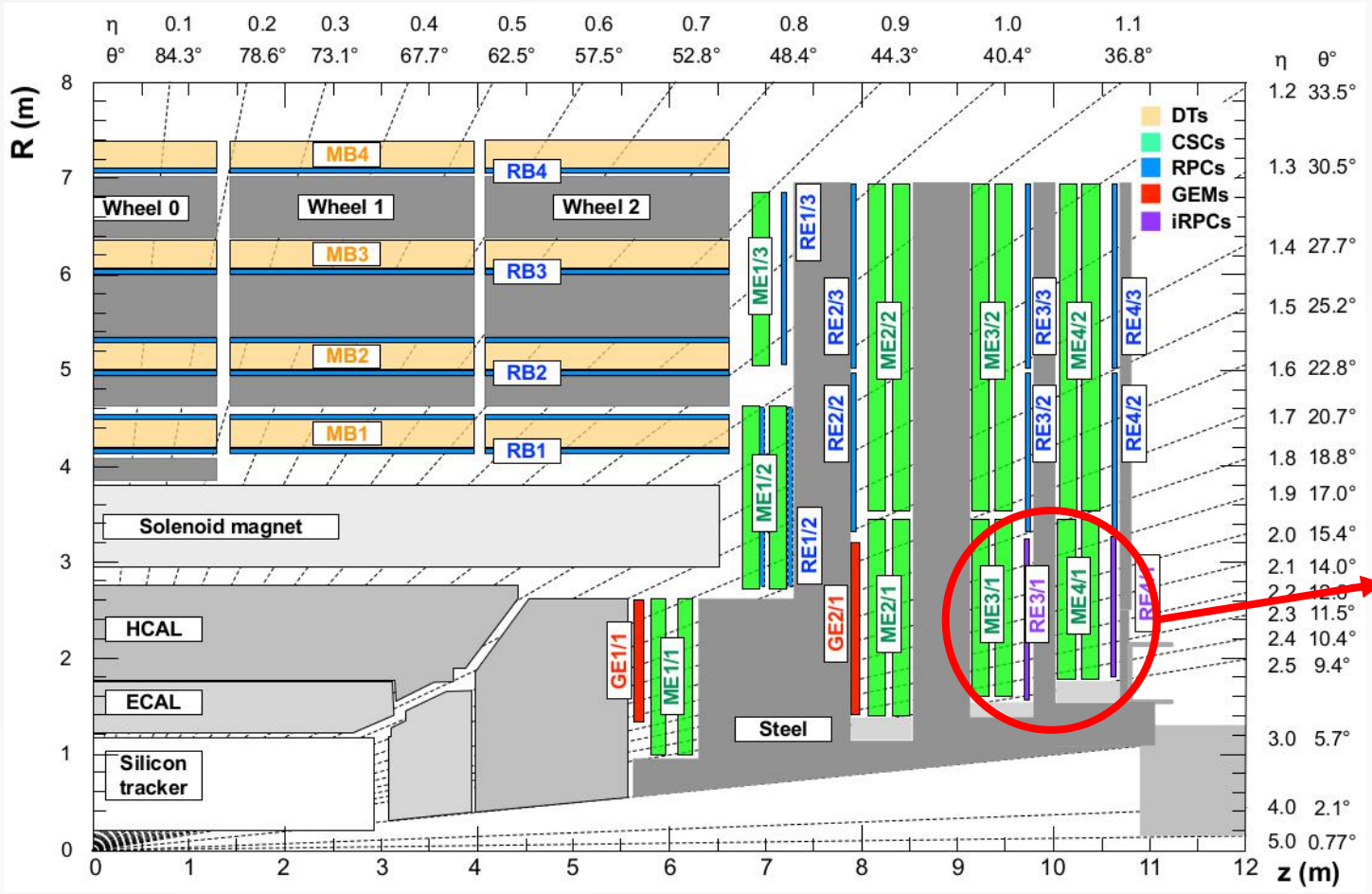
L.Mirabito on behalf of RPC group

Muon Upgrade Workshop 11-13 September 2018

RPC upgrade at high η

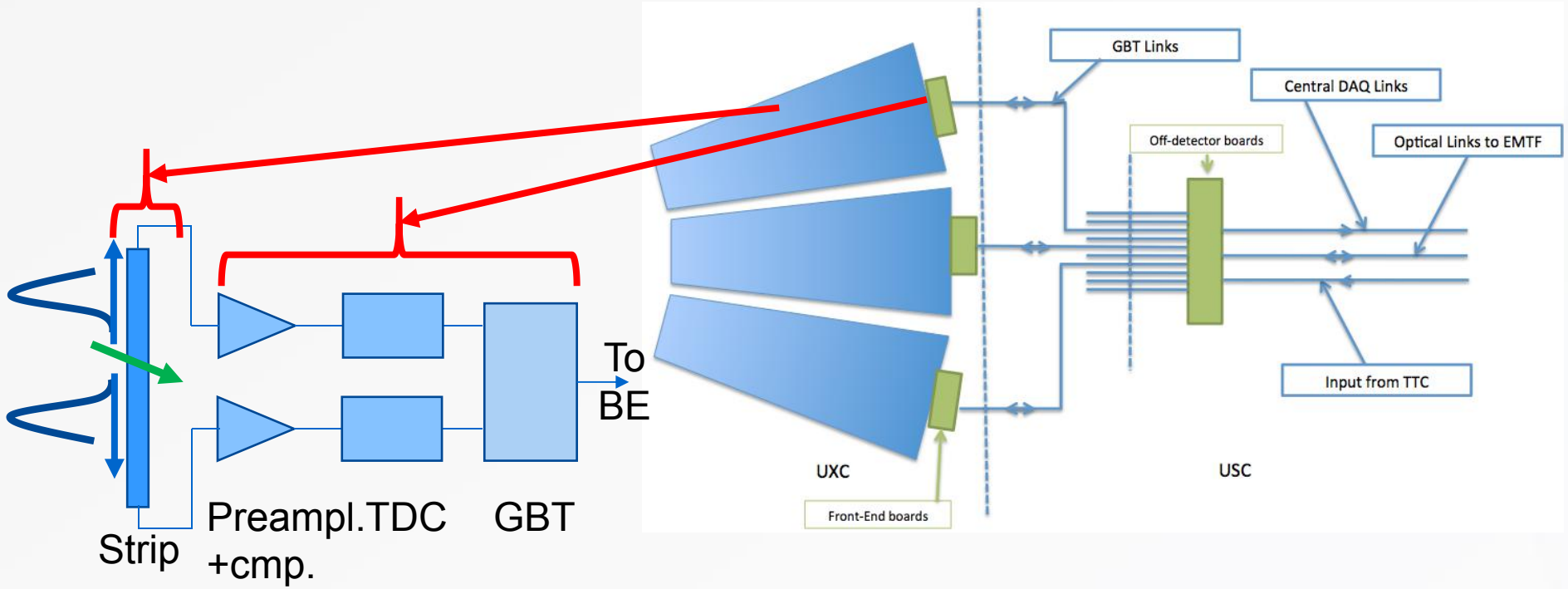
72 chambers to equip area with 1.8 < |η| < 2.4

- Add track hits in muon reconstruction
- Search for Heavy Stable Charge Particle

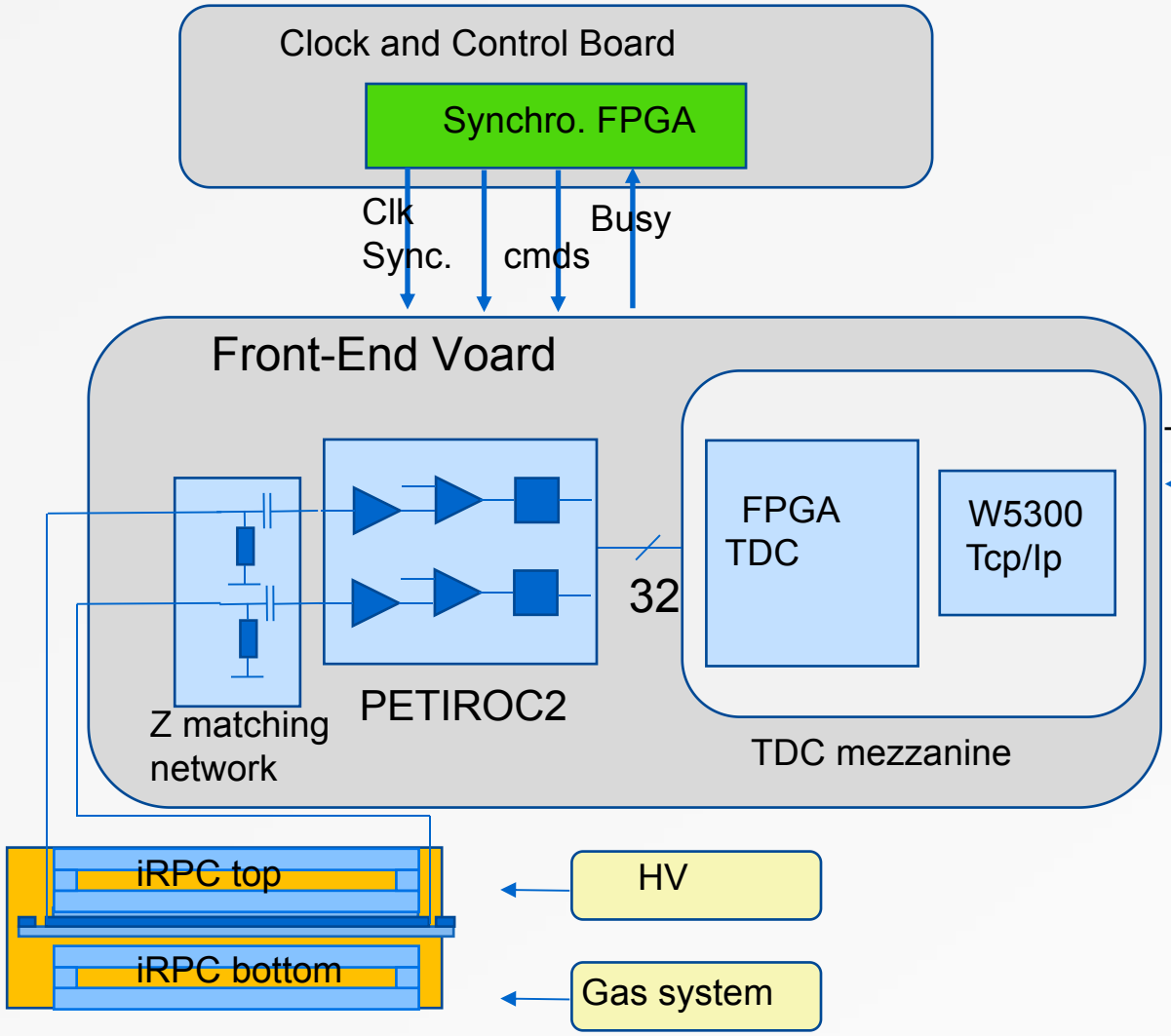


Readout Scheme

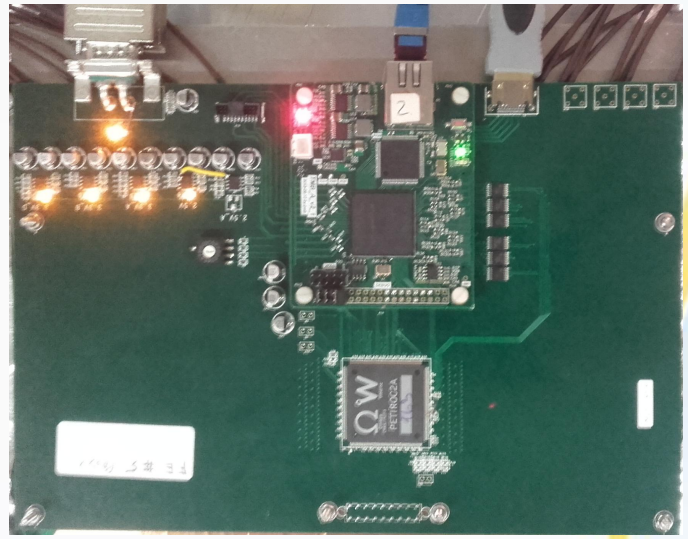
- Strip board :
  - 96 strips per chamber (1cm strip width at η = 2.8) between 2 gaps RPC
- Front-end :
  - Readout on both sides of the strip
  - Relative timing between both channels of same strip (σ~ 150 ps)
    - Position along the strip (σ ~ 1.5 cm)
- Absolute timing (σ < 1ns)
  - HSCP search



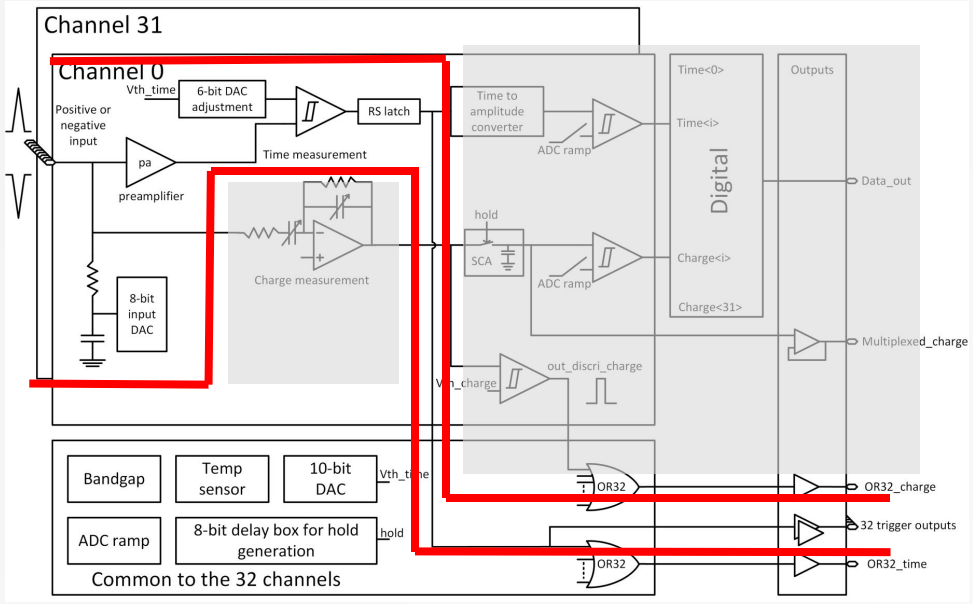
First version prototype FEBv0



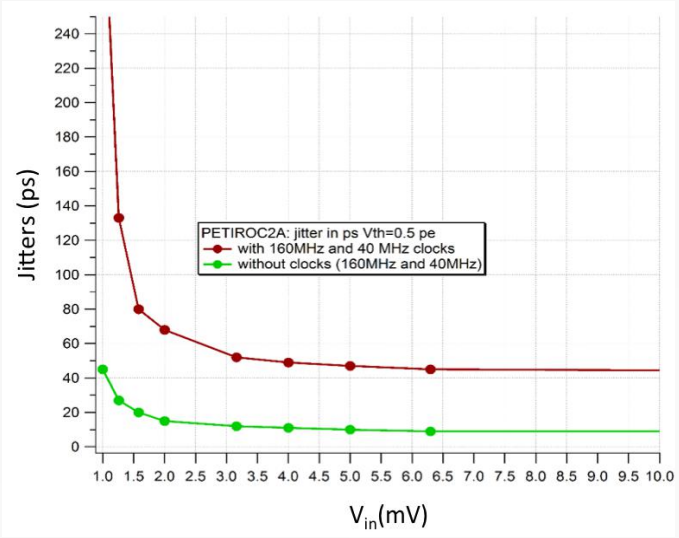
Requirements :
Fast preamp. : PETIROC2 Asic
Precise TDC : FPGA Wave union TDC

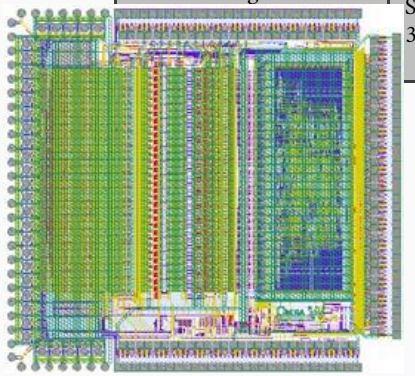


PETIROC2



Parameter	Value
Number of Channels	32
Signal Polarity	positive or negative
Sensitivity	Voltage input amplifier, 200 Ohm matching
Timing Resolution	~ 18 ps RMS on trigger output (4 photoelectrons injected)
Dynamic Range	60 fC up to 400pC
Packaging & Dimension	TQFP 208 (28x28x1.4 mm) TFBGA 353 (12x12x1.2mm)
Power Consumption	6 mW/channel
Inputs	32 analogue inputs, No external component required Inputs DC level adjustable
Outputs	32-channel trigger outputs ASIC level general trigger (OR of all channel) ASIC level second level general trigger (OR of all channels) Charge measurement (10 bits) Time measurement (10 bits)
Internal Programmable	Common trigger threshold adjustment and 6bit-DAC/channel Shaping time & gain of the charge shaper 32 x 8bit-input DAC over 1V span



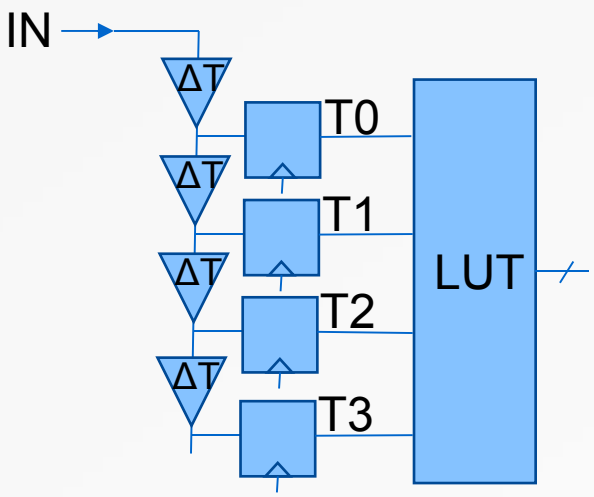


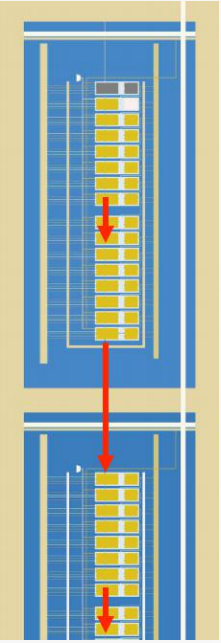
Wave Union TDC

Principle :
Input signal is propagated into a chain of identical delays (bins)

All delays output are latched on the system clock

Fine delay to clock edge is measured by position of last crossed delay element.





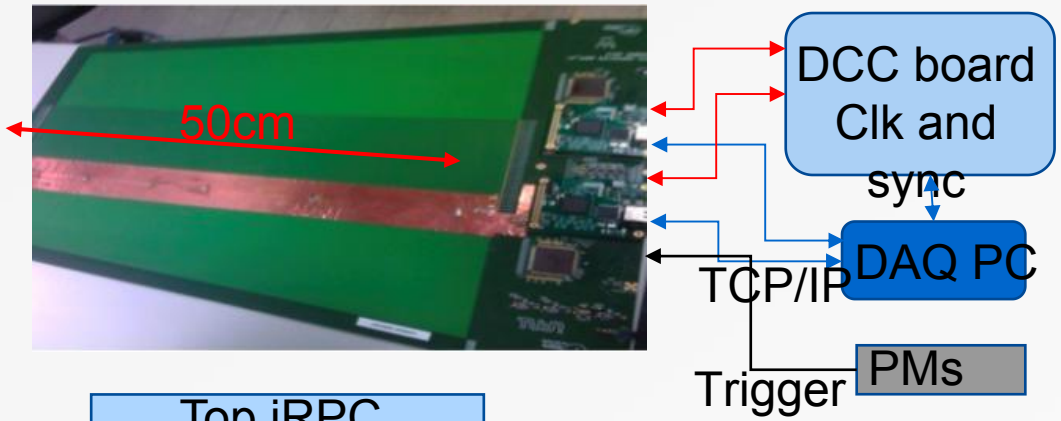
Implementation of carry chain TDC in FPGA :
Width of bins are different (Vcc and temperature). Typ. 60ps for Altera Cyclone II
Some ultra-wide bins (LAB boundary crossing). Typ. 165ps for Altera Cyclone II

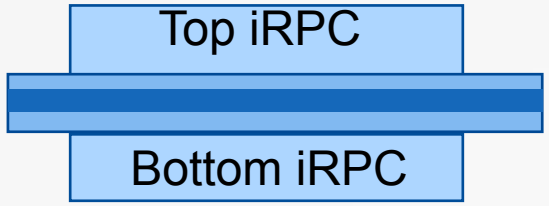
Wave union TDC solves this problem by splitting the input signal in 2 edges and ensuring that in any case, at least one edge is not in the ultra-wide bin.

Details in : QI Ji, DENG Zhi, Liu Yi-nong. Nuclear Electronics &Detection Technology, 2011, 31(4): 378-381.

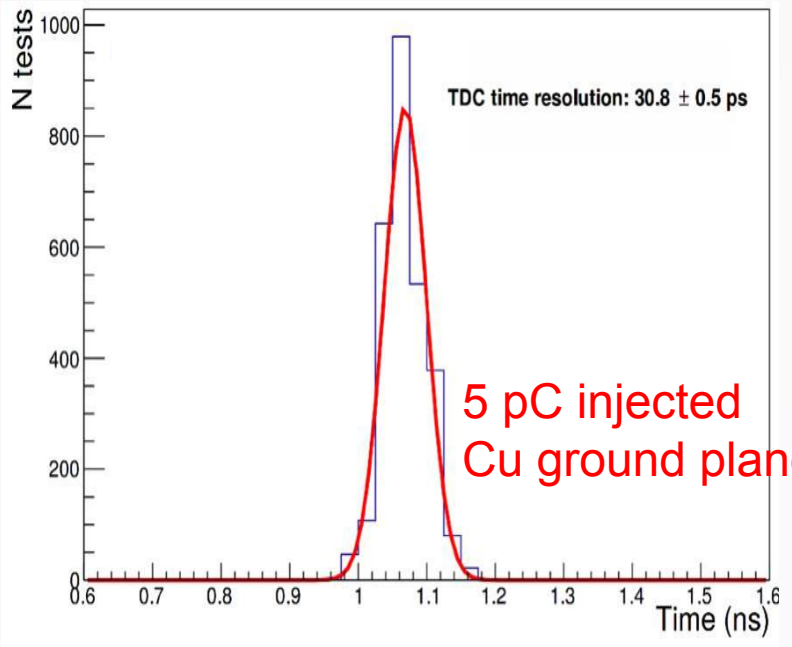
2017: Test of small size PCB's

- 32 x 50cm strips (3,5mm pitch) and 32 off detector return lines (1mm wide)
- 2 iRPC chambers : 1.4/1.4 mm and 1.6/1.6 mm
- 2x Petiroc ASIC and 2x Wave union TDC mezzanine

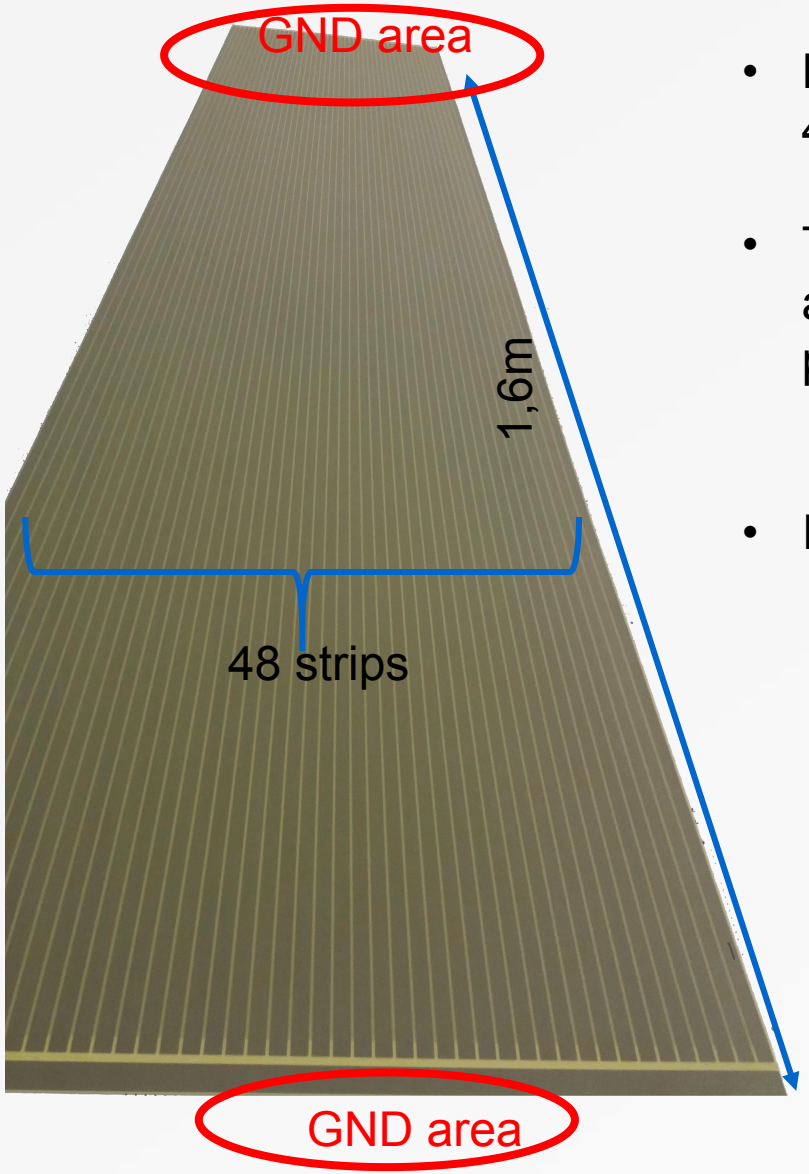




Pcb with buried strips, readout on both sides



2018: Real size PCB prototypes



- Each strip PCB covers half of a cassette with 48 strips (1 cm each)
- The strip, both gaps and cassette behave as a stripline where the cassette is the ground planes
  - Fine impedance adaptation needed
- Impedance of the strip is defined by :

$$Z_c = \sqrt{\frac{R_s + j.L_s.\omega}{G_p + j.C_p.\omega}}$$

Where :
R_s : Resistance
L_s : Inductance
G_p : Conductance
C_p : Capacitance

PCB impedance measurements

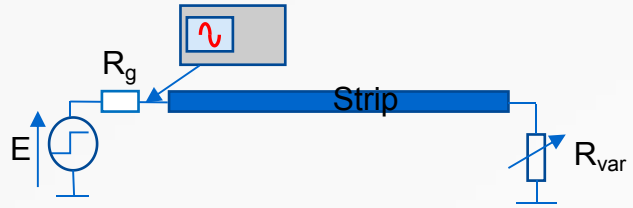
To minimize signal reflections, the stripline impedance must be controlled up to the asic.
3 methods were used to measure strip impedance :

- **Direct measurement of line parameters with a RLC meter (at 2MHz)**

Side	C_p (pF)	G_p (µS)	L_s (nH)	R_s (mΩ)	Z_c (Ω)
Wide	244	934	482	467	**43,5**
Narrow	244	934	487	461	**44**

- **Direct measurement with potentiometric line adaptation**

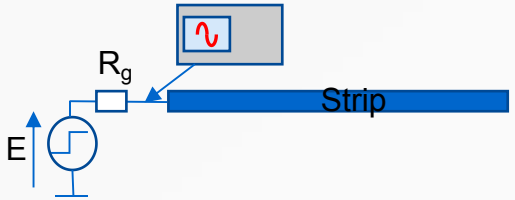
Z_c= 46 Ω



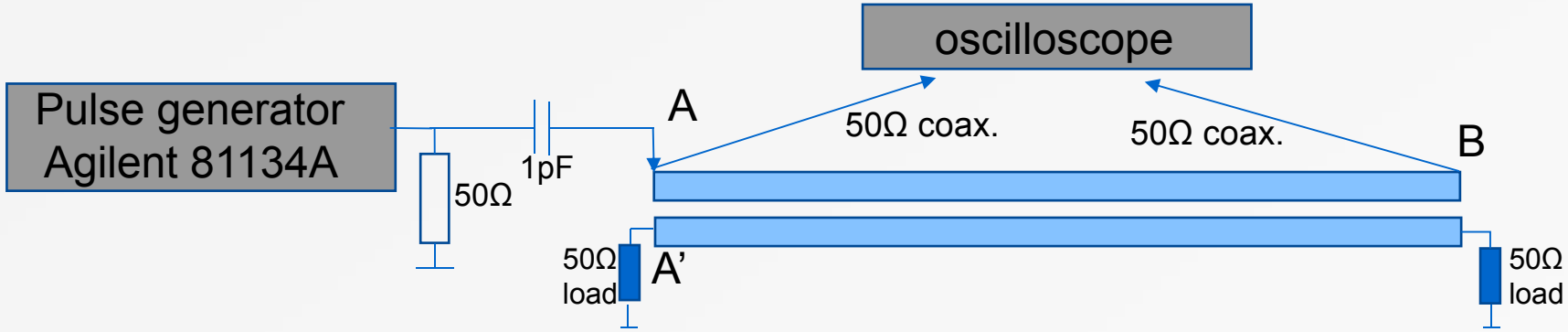
- **Reflection Method**

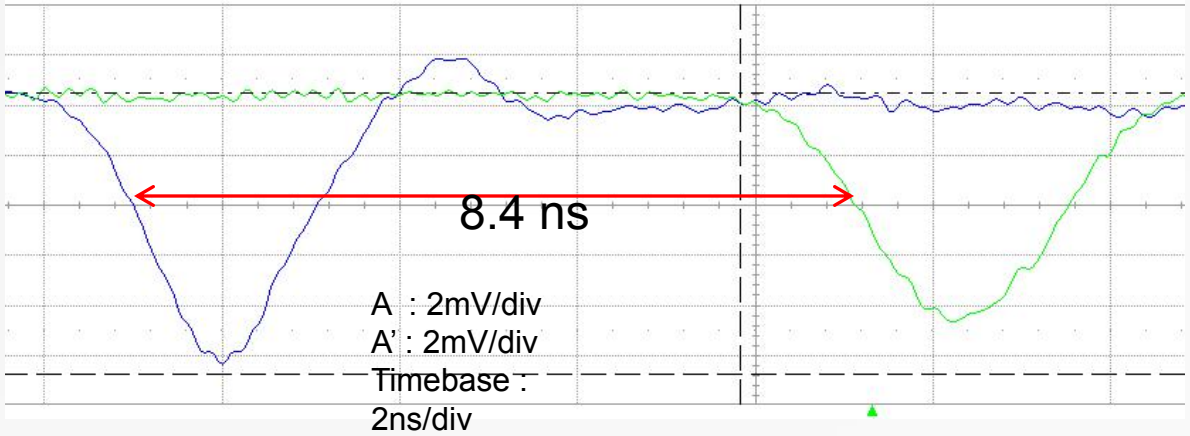
$$Z_c = \frac{R_g . V_s}{E - V_s}$$

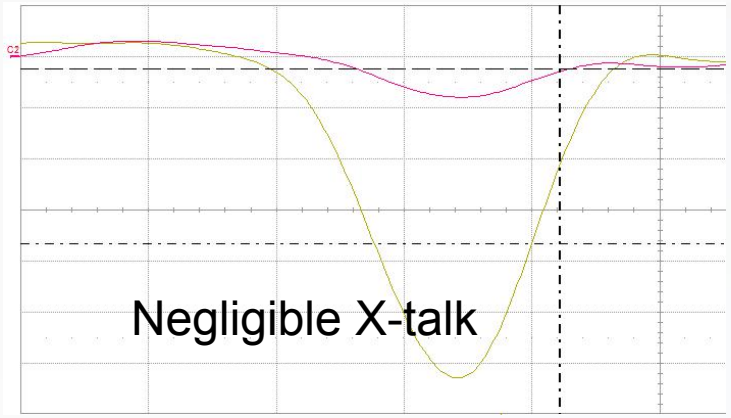
Z_c=41Ω



Pulse shapes



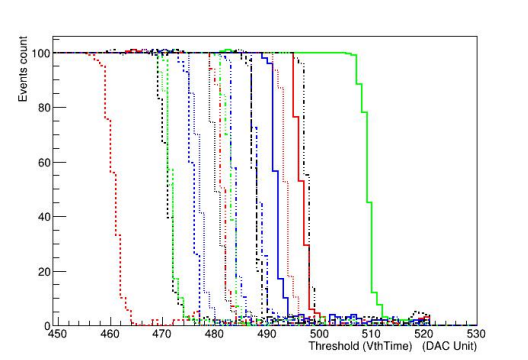


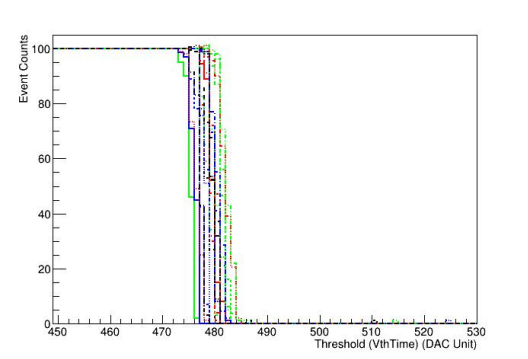


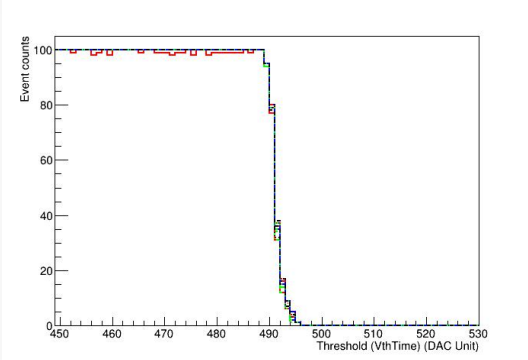
2018 prototypes

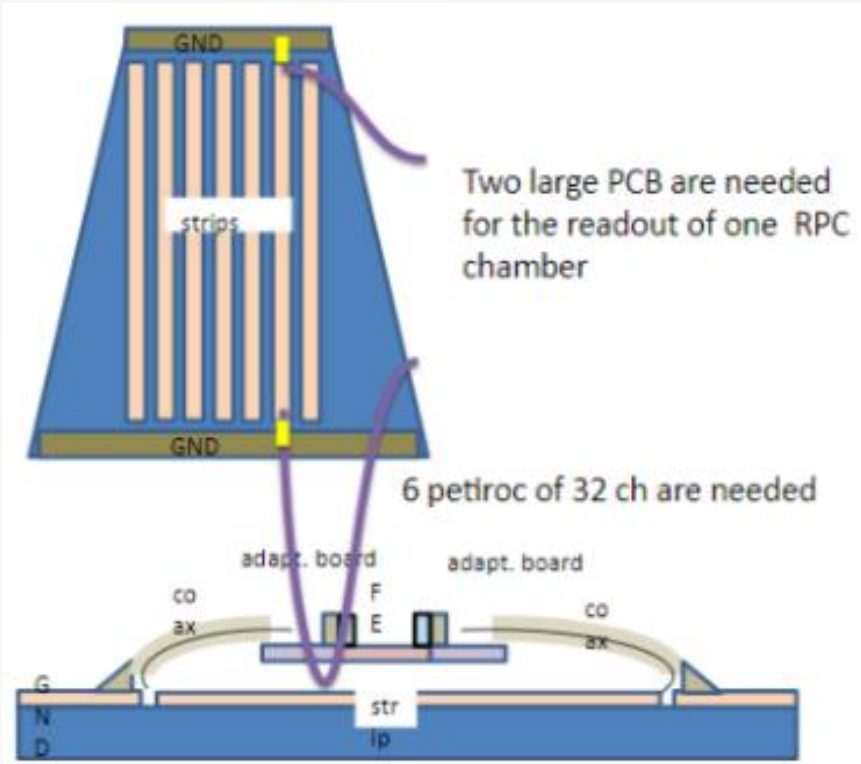
- **Challenge**:
  - Build a thin (2 x 300 microns + Cu) , large (50x160) PCB.
  - Very few producers identified
- **Two designs tested**
  - Optimal solution: Return lines embdedded in the PCB
    - Tuned Z adaptation, easy mechanical integration, shielding
    - loss of few (~ 5) cm at large radius, 4 layers PCB
  - Backup solution: Coaxial cable connection to FEBs
    - 3 layers PCB, easy for debugging stage
    - Not perfect Z adaptation, cabling & integration (mechanics,shielding) issues
- Two test beams in GIF++ (May & August) to validate their performances

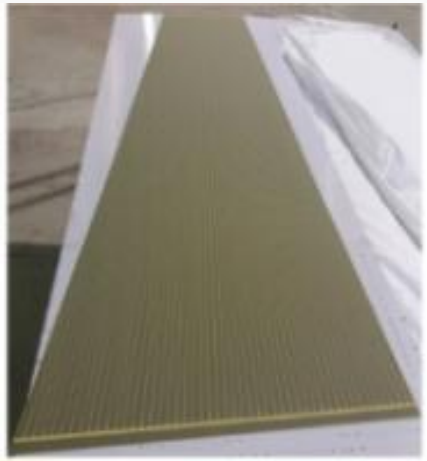
Coaxial cable version





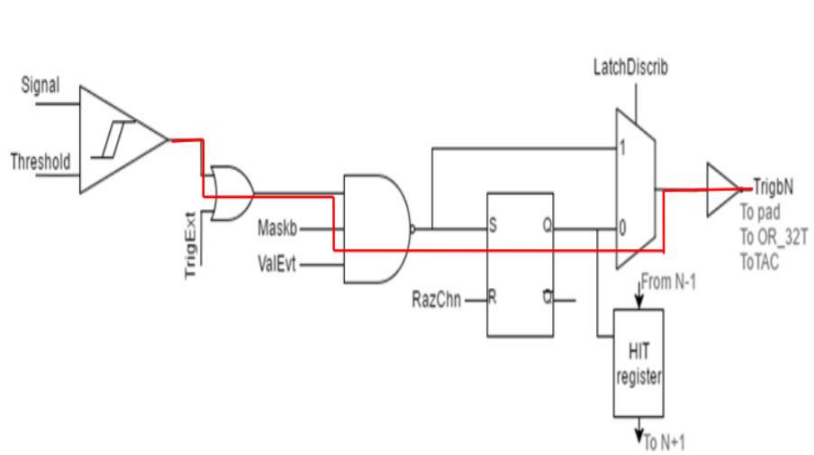


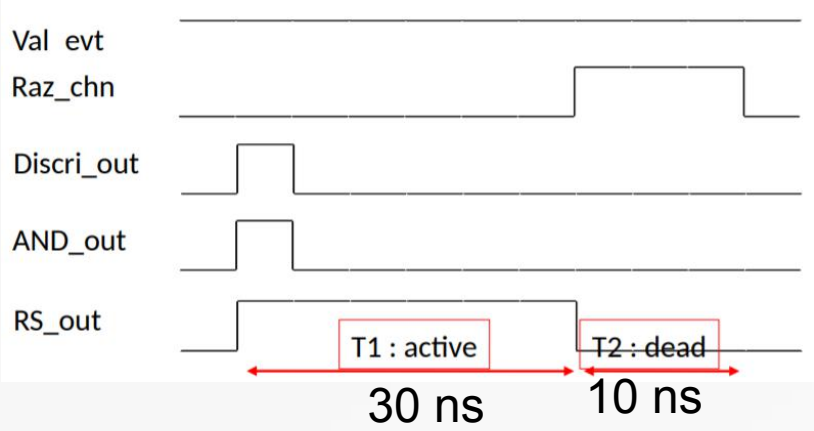


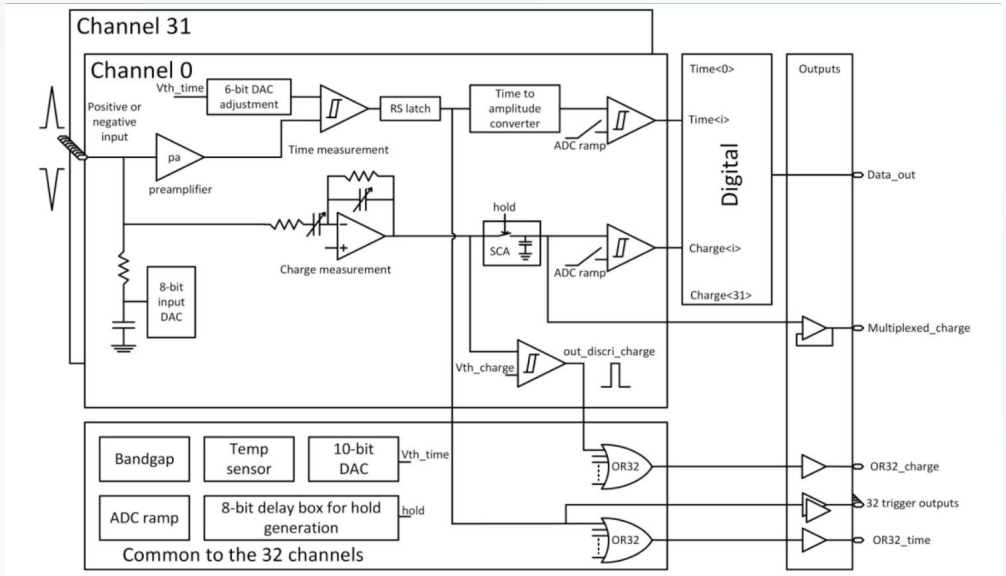


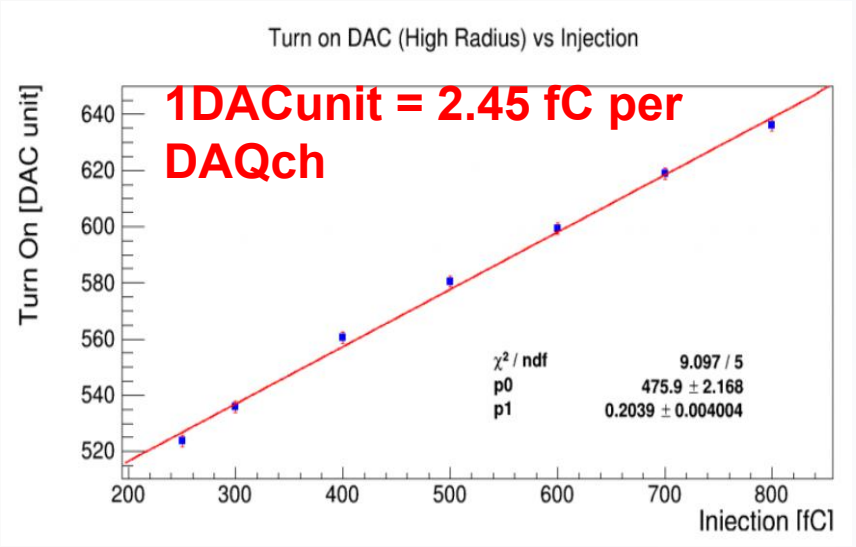
- Noise pickup, re-trigerring -> Shift of the turn on
- Acquisition window for pedestal 5 micros
- Threshold set much higher to limit tail effects on large time windows and keep acceptable rate
- Threshold used: 524(DAC)-480(DACu) = **44 DACu = 107.8 fC**

Electronic tuning: Calibration & retrigerring control



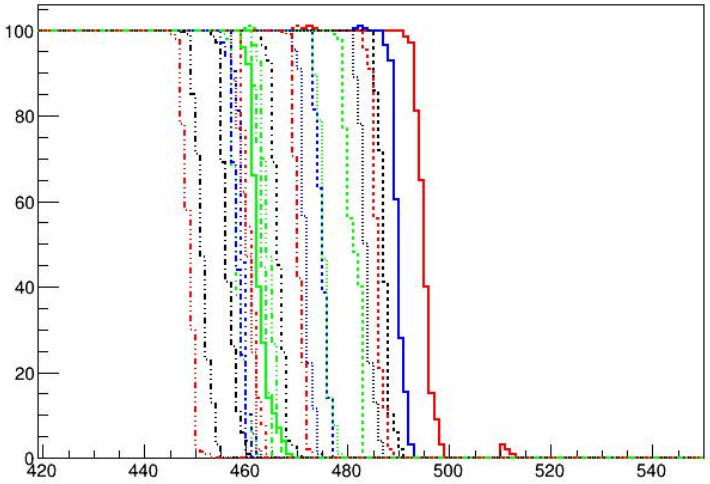


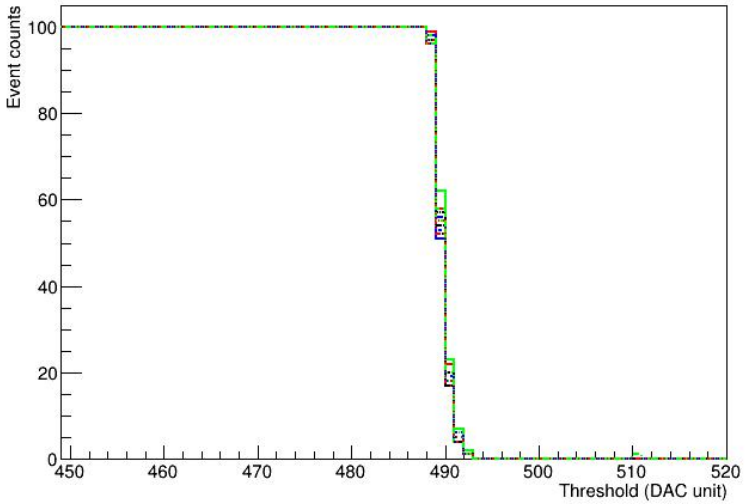


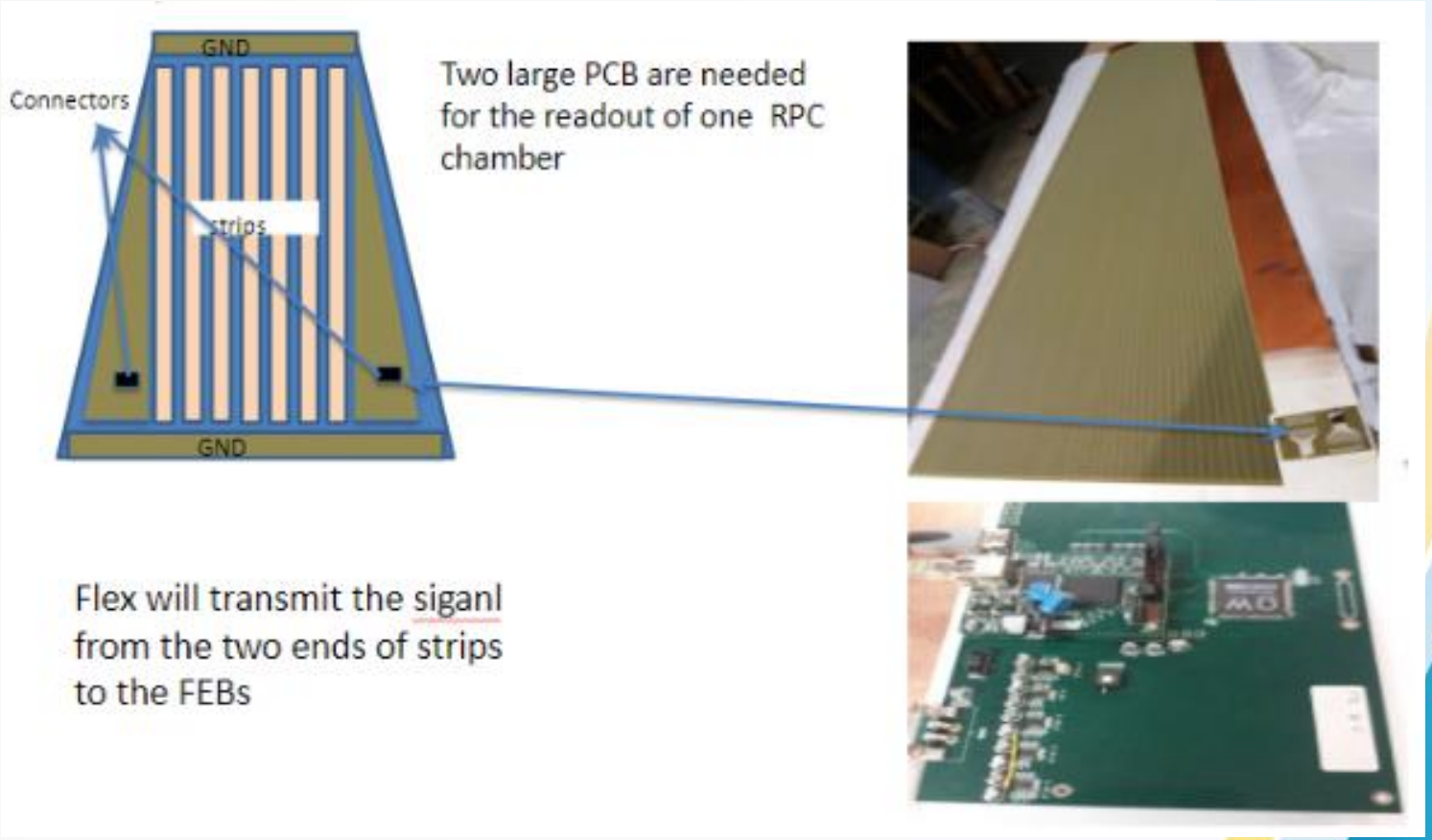


- *Current setting:* Latched with deadtime = 10ns;
- ~3% loss of efficiency for 2 kHz/cm² mean background rate in the FEB @ HL-LHC (600 Hz/cm² expected with a safety margin of 3).

Return lines version

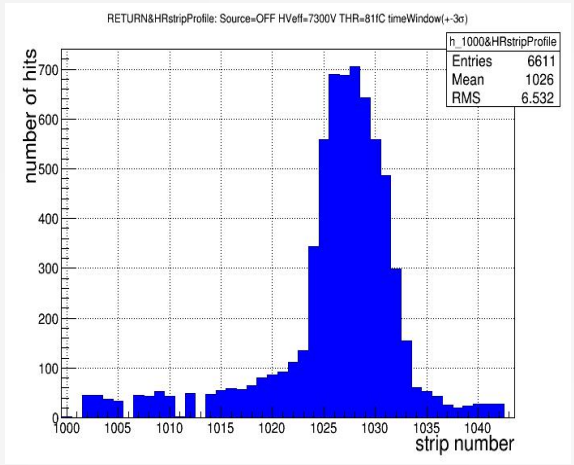


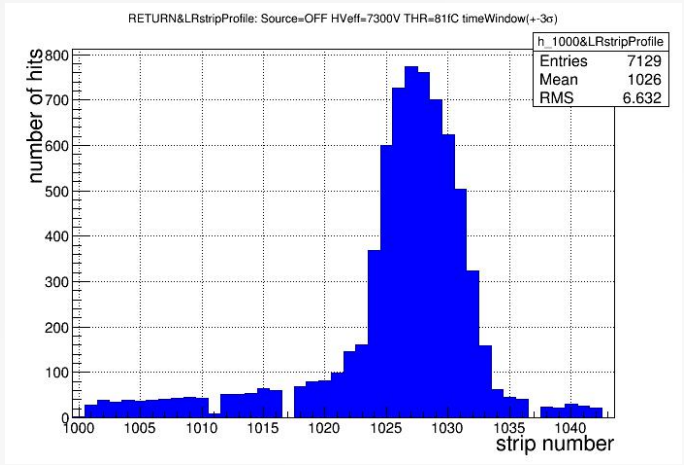


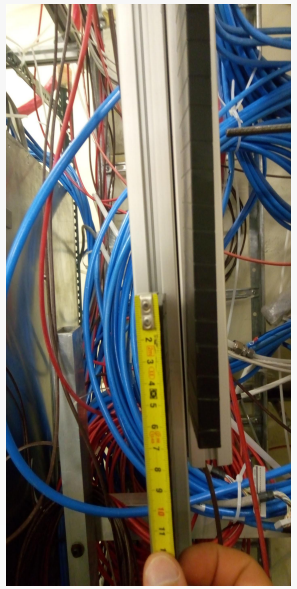


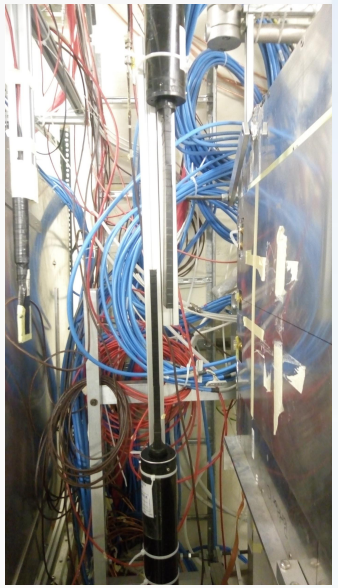
- Less Noise pickup
- Threshold used: 513(DAC)-480(DACu) = **33 DACu = 81 fC**

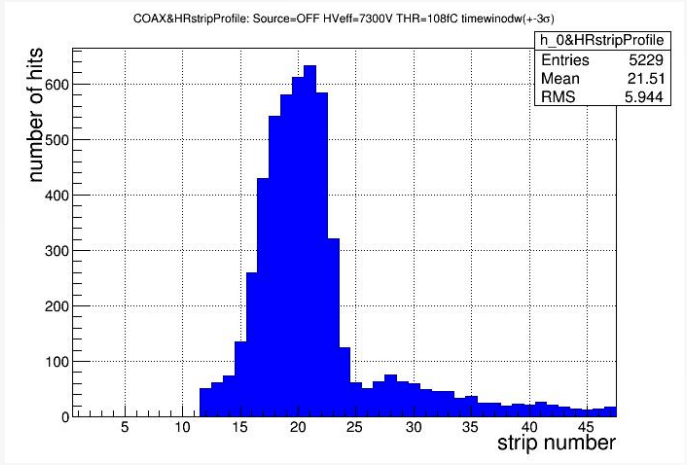
GIF++ setup (August 2018)

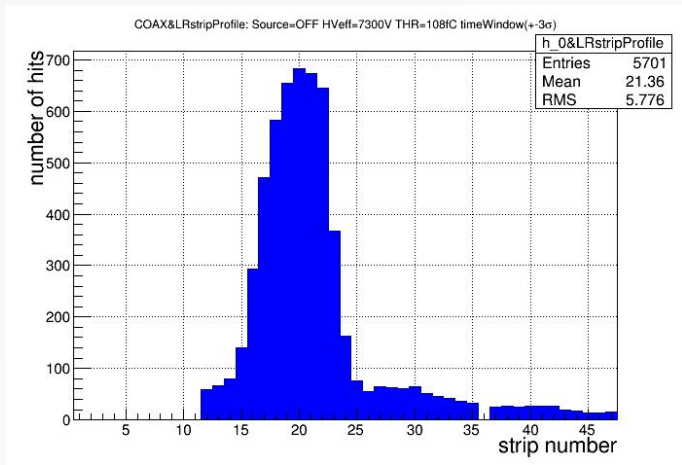


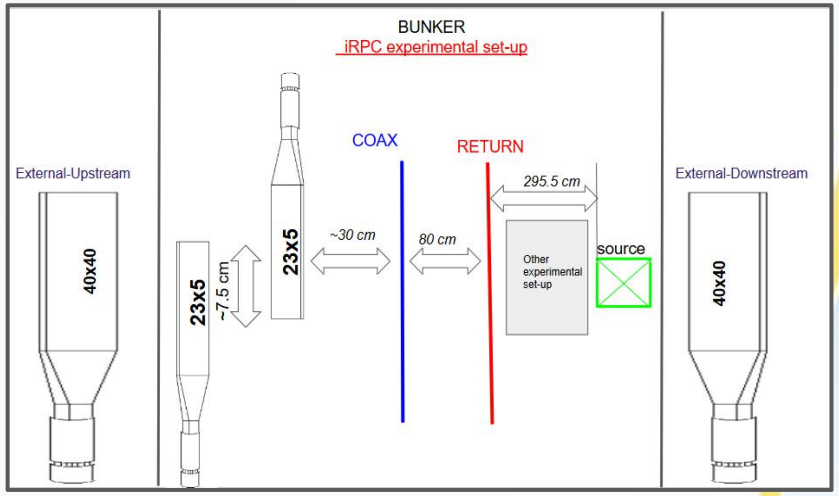






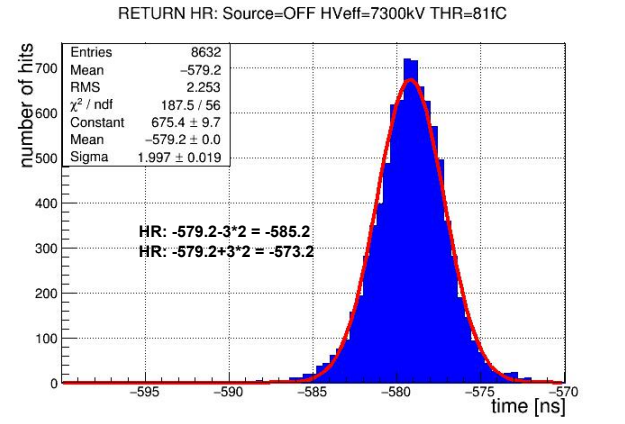




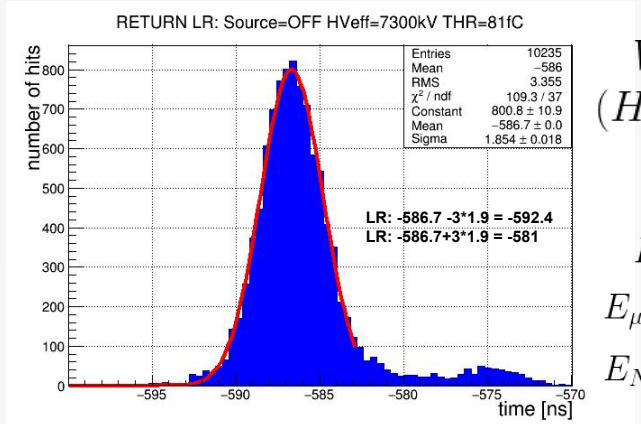


Time selection & efficiency

RETURN HR: [-585.2; -573.2]



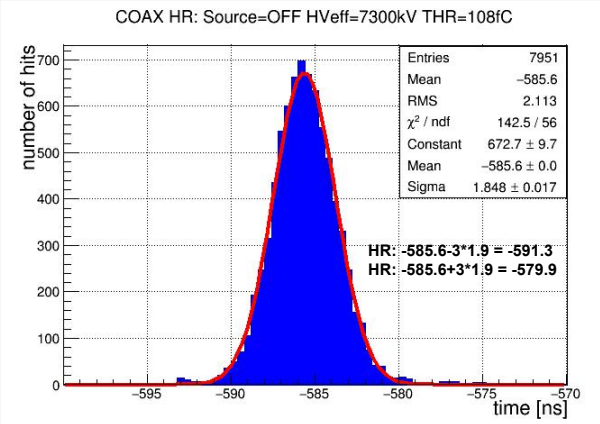
RETURN LR: [-592.4; -581]



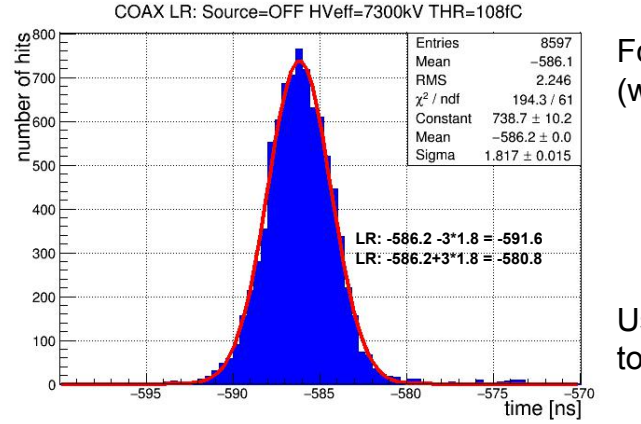
$$WP = HV_{95\%} + 150V$$
$$(HV_{95\%} : HV_{eff}\ the\ \varepsilon\ is\ 95\%\ of\ \varepsilon_{max})$$

$$E_\mu = \frac{E - E_N}{1 - E_N},\ where$$
$$E_\mu - muon\ efficiency;$$
$$E_N - noise\ efficiency;\ E - \frac{N_\mu + N_N + N_{(N+\mu)}}{n}.$$

COAX HR: [-591.3; -579.9]



COAX LR: [591.6; -580.8]



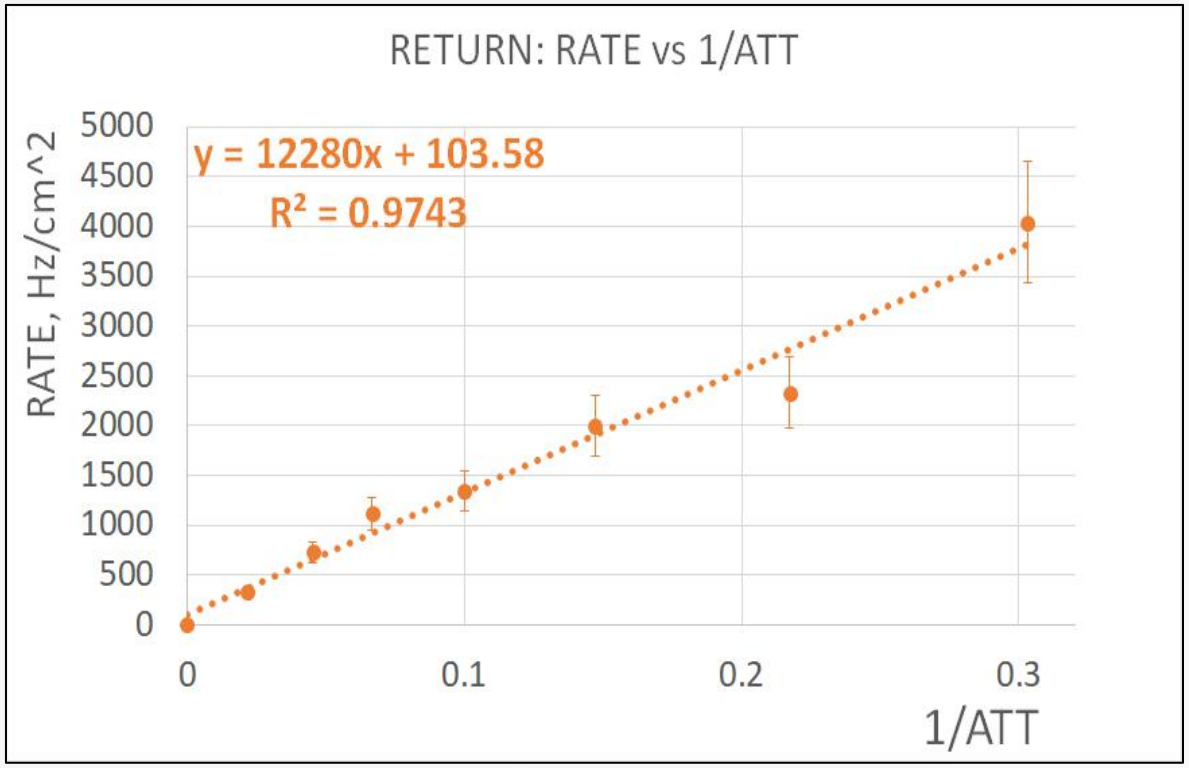
For each run calculate time interval (windows) with the following way:

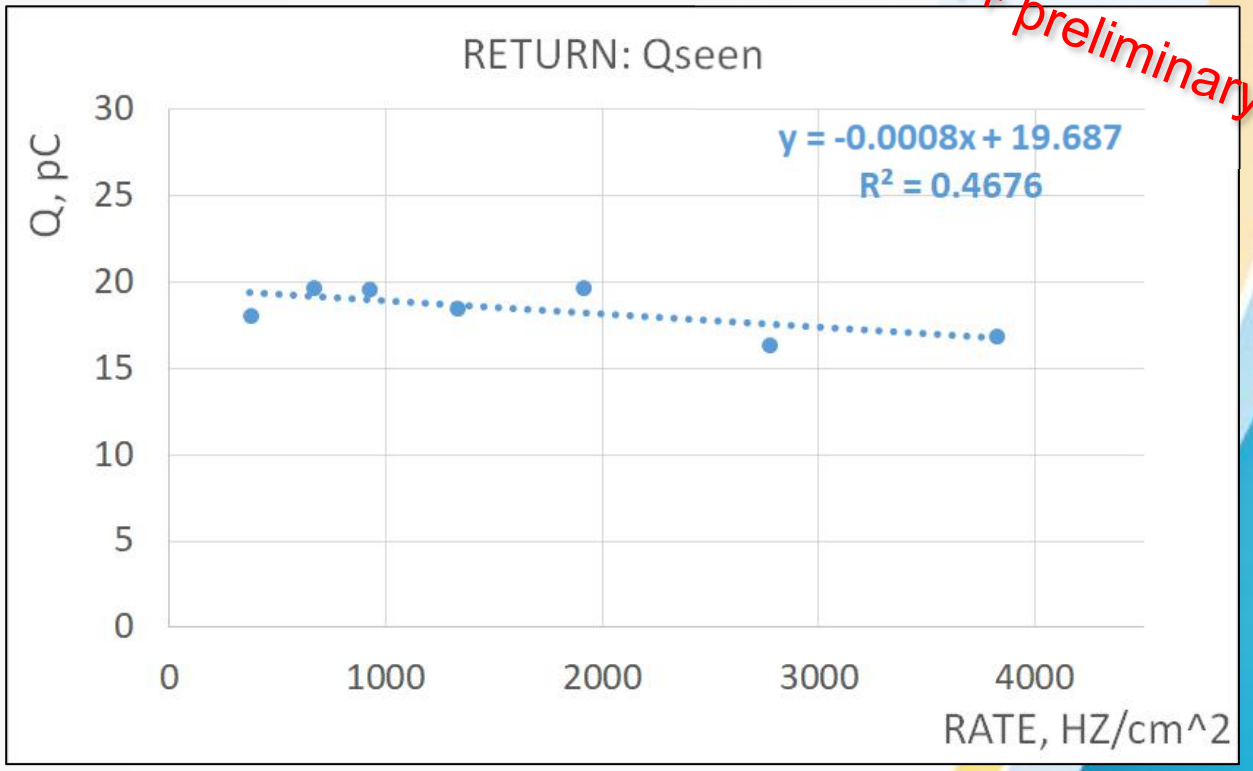
- Find the beam area;
- Fitting distribution inside this area with guess function;
- Choose window: +-3 sigma from a mean value of the fit function.

Use the same size of time window but shift it to 200ns for estimate rate.

Rates & total charge seen (Return lines chamber)

CMS GIF++ preliminary

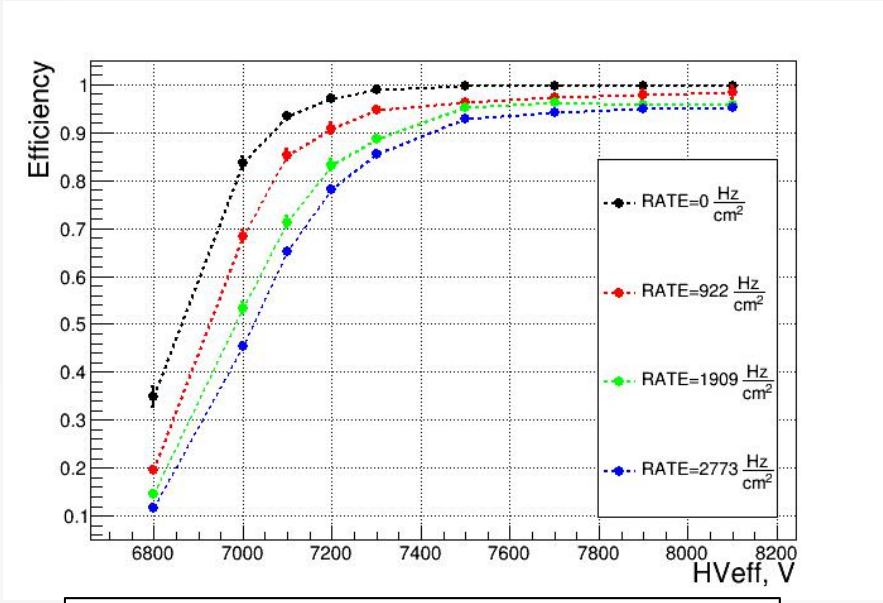


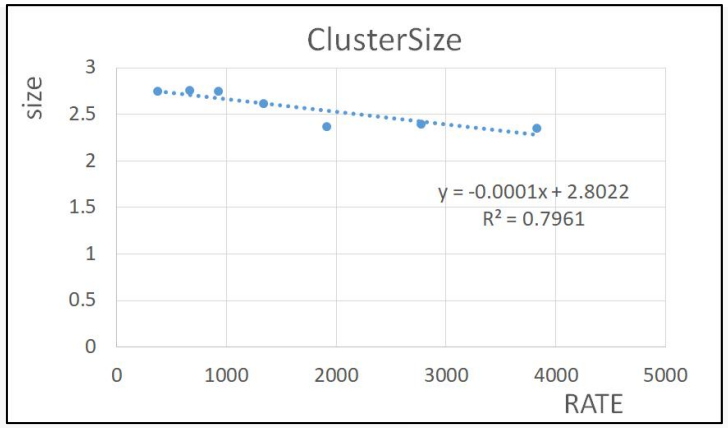


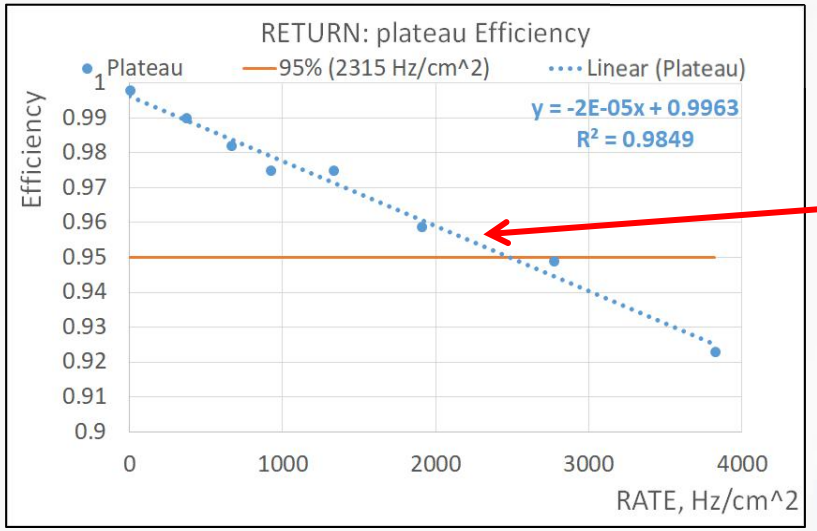
- Minimal $Q_{seen}{}^{\gamma} = (I_{top}+I_{bottom})/Rate/Surface = Q_{Slow} + Q_{Fast}$ (~1/12.)
- $Q_{seen}{}^{MIP} = 1/2\ Q_{seen}{}^{\gamma}$ (*MIP interacts in the 2 gaps)* ~ 10 pC
- Coherent with threshold settings

Performances (Return Chamber)

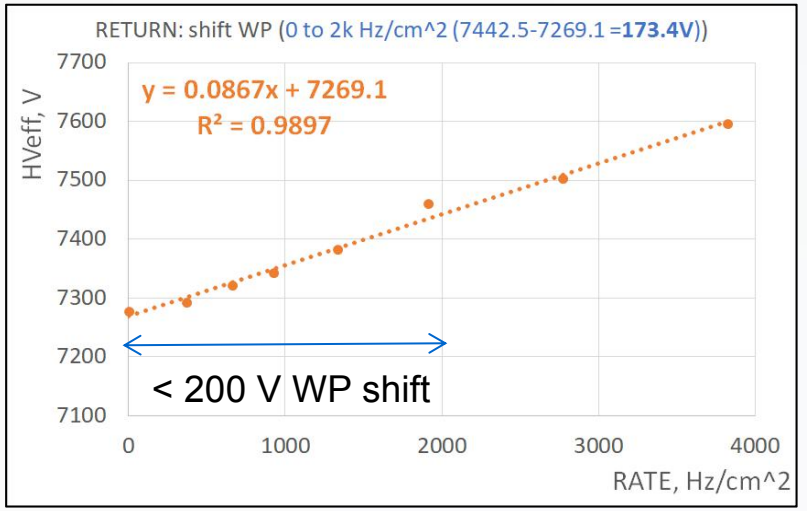
CMS GIF++ preliminary





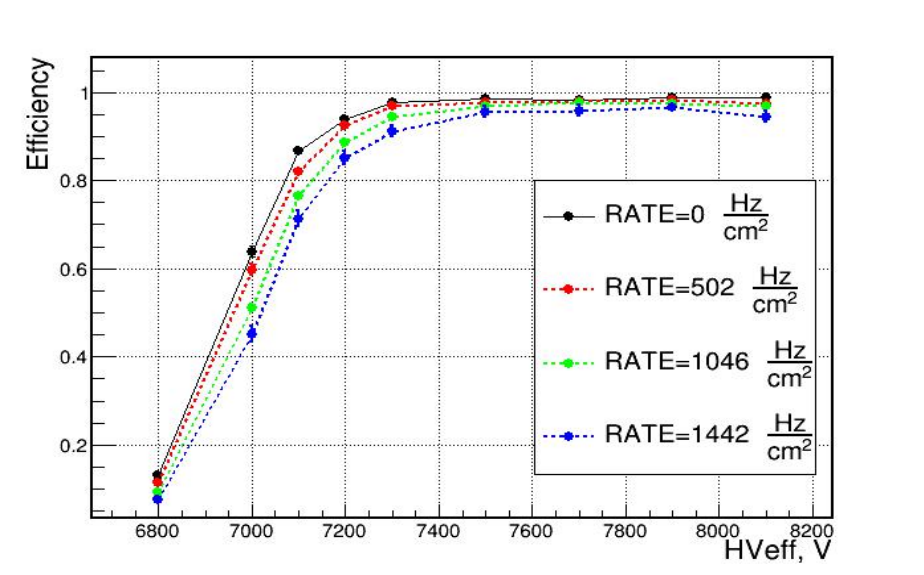


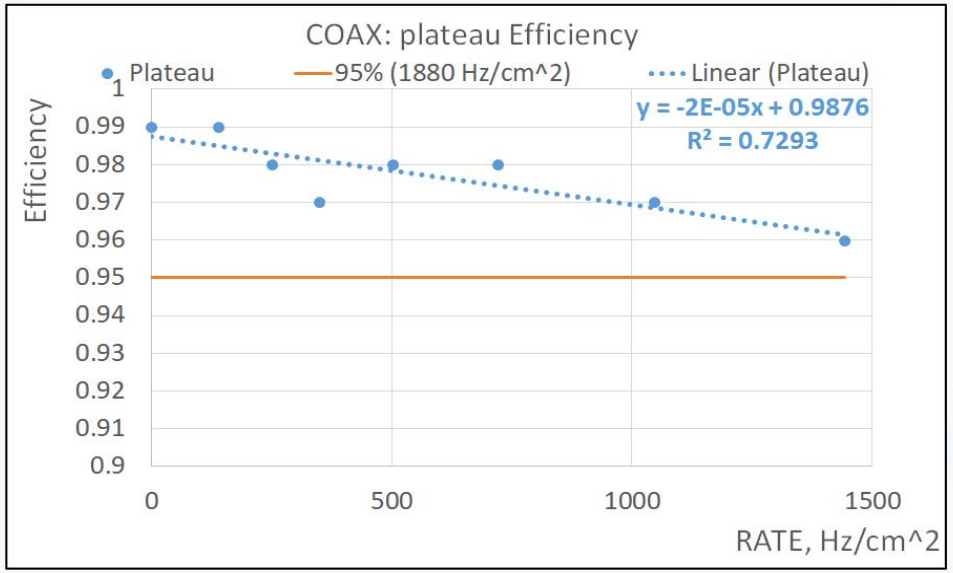
Loss mainly due to deadtime at high mean rate

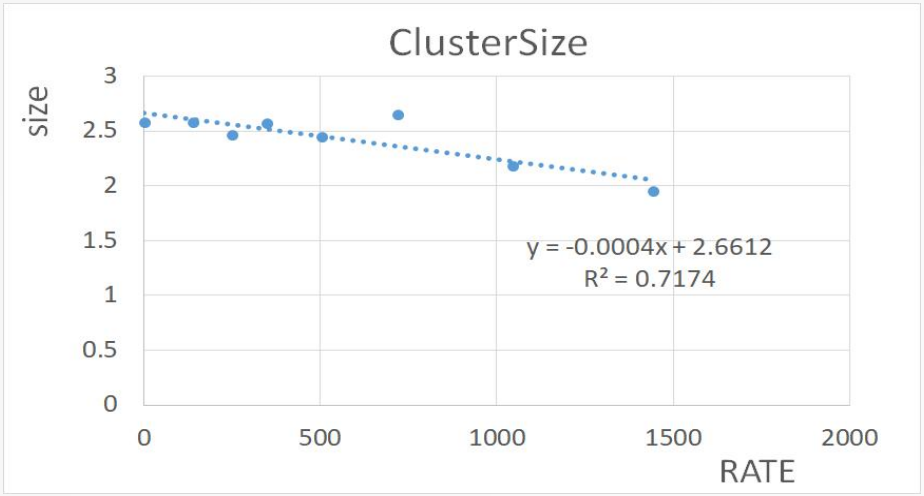


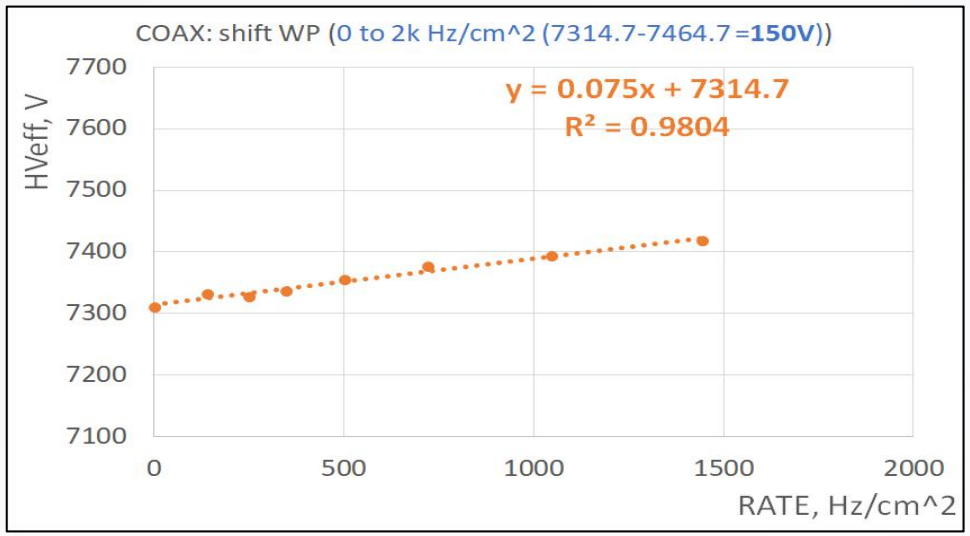
Performances (Coaxial cables chamber)

CMS GIF++ preliminary



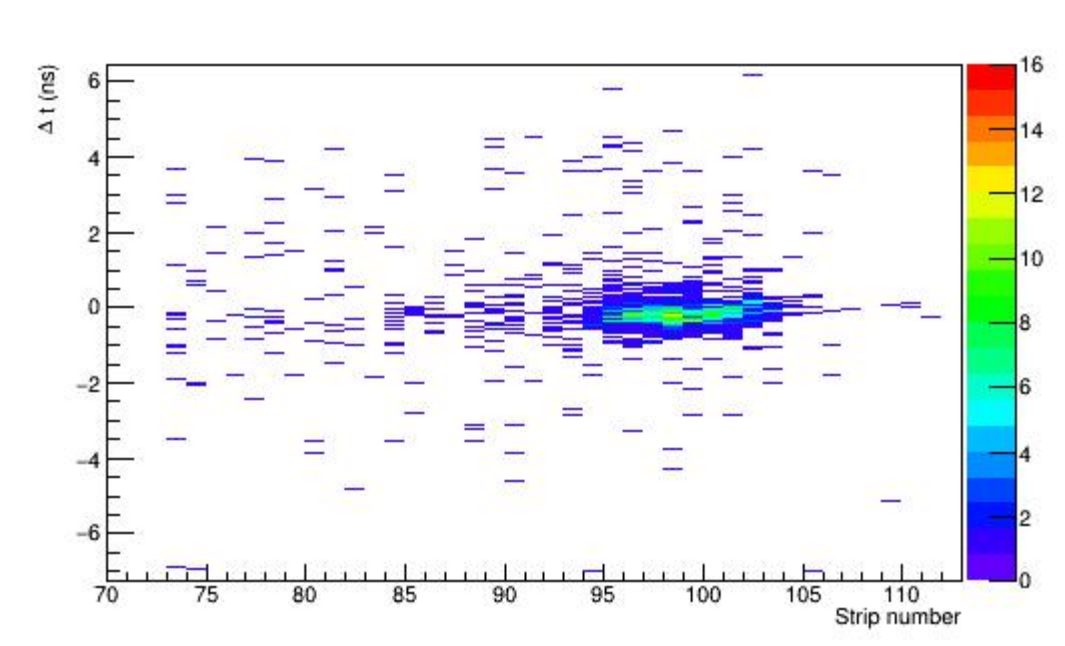


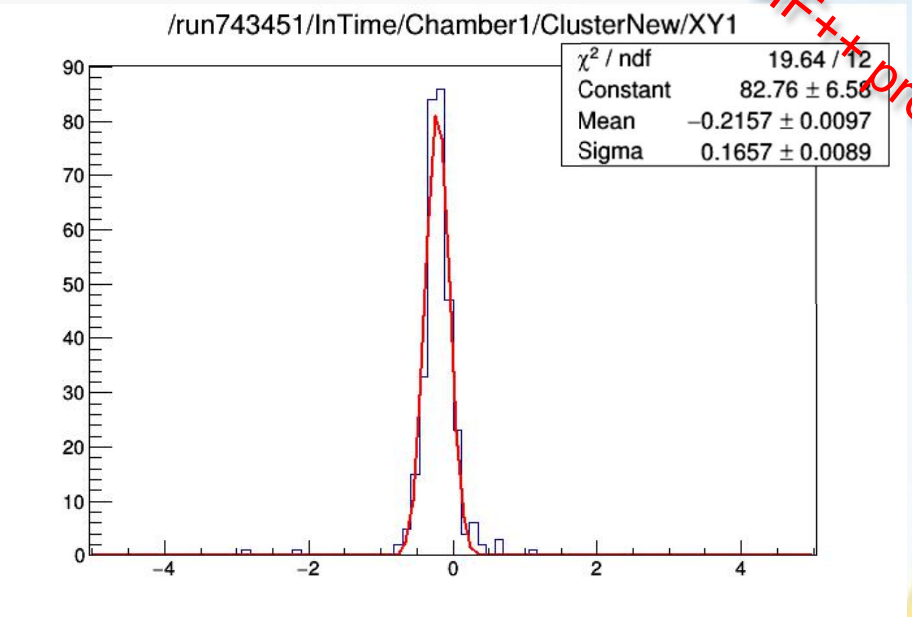


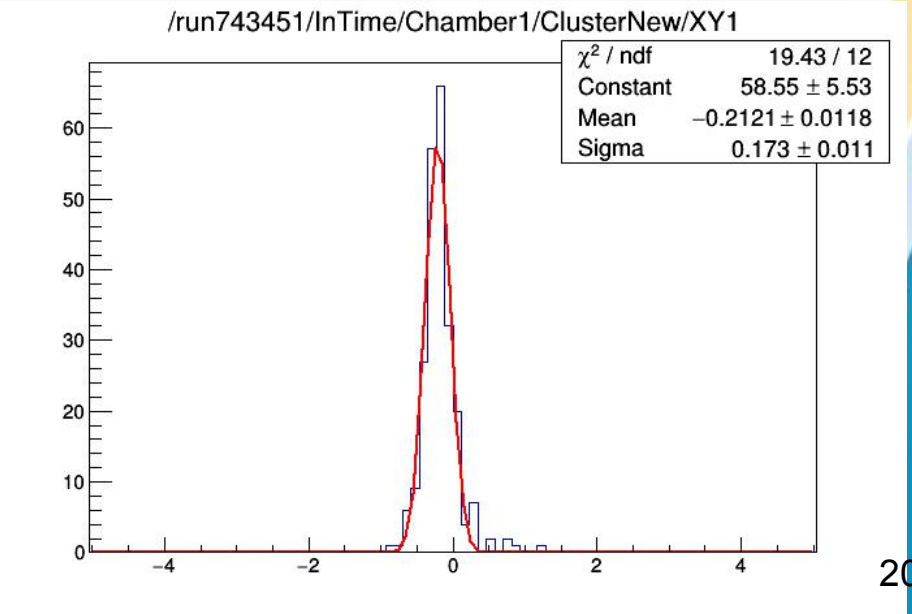


Position reconstruction

- Cluster algorithms includes
  - Strip vicinity
  - Δ t compatibilty
  - Time Of Arrival compatibility
- σ (Δt) ~ 170 ps ⇒ 0.17/2 *160./8.4 ~ 1.6 cm
  - Rough alignement
  - No time walk correction (edge strip rejected when possible in position evaluation)







CMS GIF++ preliminary

Summary

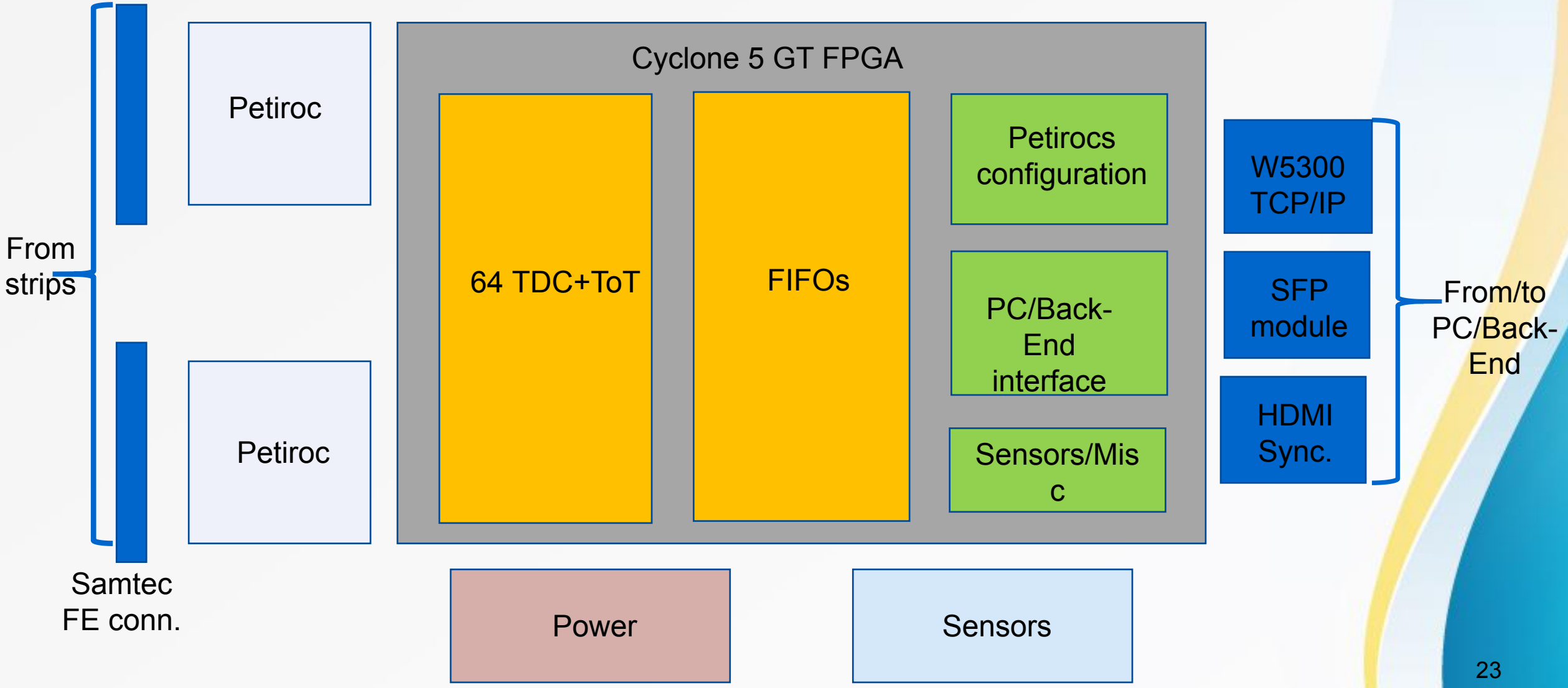
- Full size prototype tested with 2 versions of PCB's
  - Coaxial cable or embedded return lines
- Good performances achieved up to 2 kHz/cm^2 on the whole chamber
  - $\varepsilon > 95$ %
  - Working point shift bellow 300 V
  - Position resolution ~ 1.6 cm
  - PCB & ASIC performances are validated
- Two designs give comparible results but production and integration much easier with return lines design

Short term plans (Q4 2018)

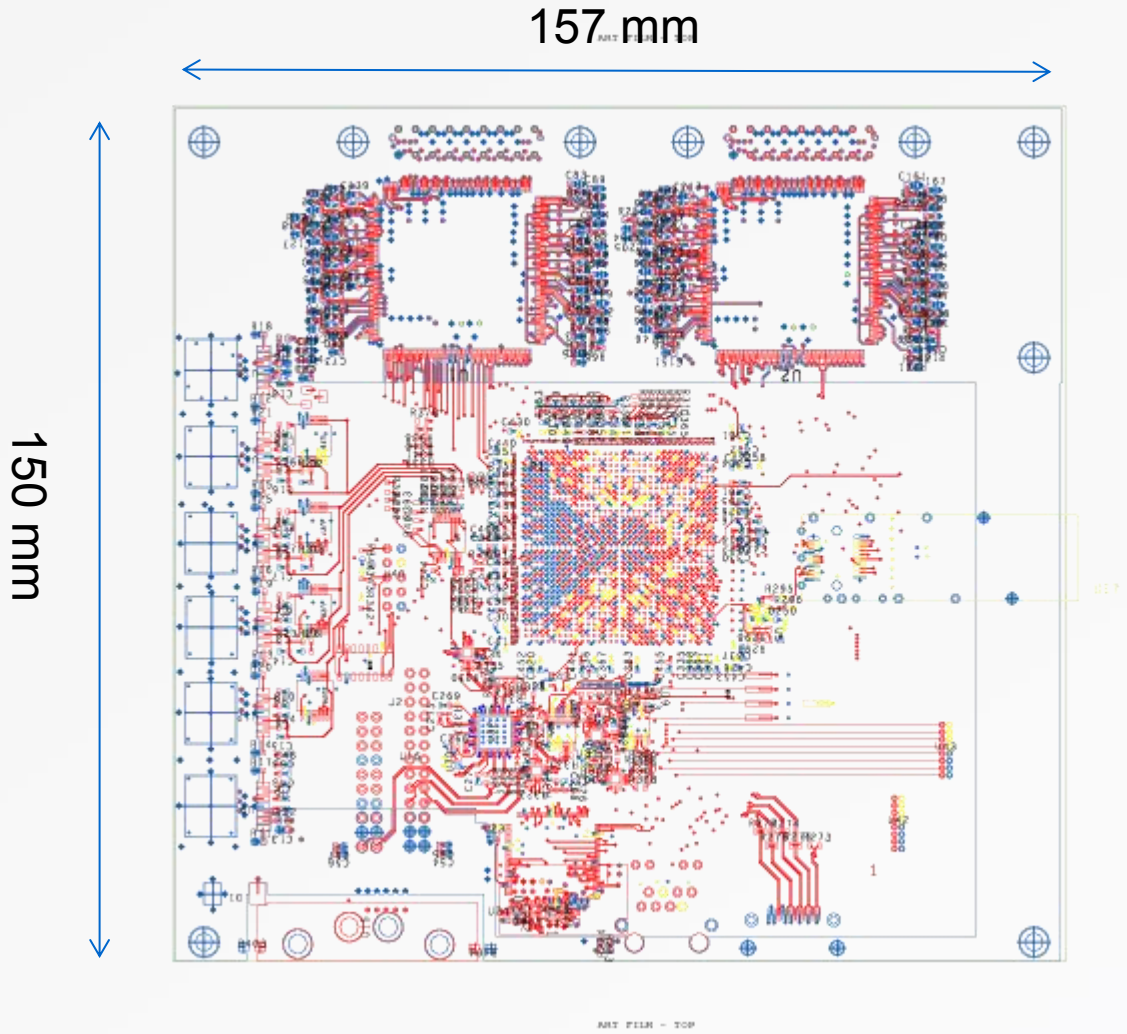
- FEBv0 limitations
  - Cyclone II FPGA: Limited space (24 channels)
    - no possibility to read a complete ASIC
    - no Time Over Threshold measurement
  - Wiznet TCP/IP readout
    - 5 Mbit/s bandwidth
  - Custom clock and command system (ILC devs)
- FEBV1, **validation of final FPGA** (cabling, expected this week)
  - Cyclone V GT
    - 64 channels read with rising & falling edge (TOT) , firmware ready
    - High speed serial link
      - GBT FPGA implementation feasible (to be done)
  - Keep Wiznet + Custom clock as backup-debug
  - GBT ⇒ TTC implementation + Back-end integration tests
  - 2 PETIROC2 chips read
  - Compatible with previous PCB's

To be tested in October GIF++ test beam

FEBv1 conceptual layout



FEBV1 layout



Further plans

- **PETIROC2B**
  - Programable capacitors added to tune pre-amplifier bandwidth
    - slower rise time ⇒ Lower threshold, still acceptable time resolution, possibly improves re-trigerring issues (?)
    - pin-2-pin compatible with PETIROC2A
  - ASIC submitted in July, waiting for foundry (<Q1 2019?)
- **Final FEB** (< Q2 2019)
  - 1 FEB per PCB (1/2 chamber)
  - 3 PETIROC2+ Cyclone V TDC blocks
  - 1 FPGA for communication (GBT link)
  - Final LV connectors
  - Integration with back-end prototype(s)
- **Neutrons test** (< Q2 2019)
  - Mainly firmware performances

Final FEB conceptual layout