0.1 Overview

The Resistive Plate Chambers (RPC) system, located in both barrel and endcap regions, provides a fast, independent muon trigger with a looser p_T threshold over a large portion of the pseudorapidity range ($|\eta| < 1.6$) [add reconstruction].

During High-Luminosity LHC (HL-LHC) operations the expected conditions in terms of background and pile-up will make the identification and correct P_T assignment a challenge for the Muon system. The goal of the RPC system is to provide additional hits to the Muon system with precise timing. All these informations will be elaborated by the trigger system in a global way enhancing the performance of the trigger in terms of efficiency and rate control.

The RPC Upgrade is based on two projects: an improved Link Board System and the extension of the RPC coverage up to $|\eta| = 2.4$. [FIXME 2.4 or 2.5?]

The Link Board system, that will be described in section 0.2, is responsible to process, synchronize and zero-suppress the signals coming from the RPC front end boards. The Link Board components have been produced between 2006 and 2007 and will be subjected to aging and failure in the long term. The upgraded Link Board system will overcome the aging problems described in section 0.3.4 and will allow for a more precise timing information to the RPC hits from 25 to 1ns.

The extension of the RPC system up to $\eta = 2.1$ was already planned in the CMS TDR [ref cmstdr] and staged because of budget limitations and expected background rates higher than the rate capability of the present CMS RPCs in that region. An extensive R&D program has been done in order to develop an improved RPC that fulfills the CMS requirements. Two new RPC layers in the innermost ring of stations 3 and 4 will be added with benefits to the neutron-induced background reduction and efficiency improvement for both trigger and offline reconstruction.

0.2 The present RPC system

The RPC system is organized in 4 stations called RB1 to RB4 in the barrel region, and RE1 to RE4 in the endcap region. The innermost barrel stations, RB1 and RB2, are instrumented with 2 layers of RPCs facing the innermost (RB1in and RB2in) and outermost (RB1out and RB2out) sides of the DT chambers. Every chamber is then divided from the read-out point of view into 2 or 3 η partitions called "rolls". The RPC system consist of 480 barrel chambers and 576 endcap chambers. Details on the geometry are discussed in the paper [ref to geo paper].

The CMS RPC chamber is a double-gap, operated in avalanche mode to ensure reliable operation at high rates. Each RPC gap consists of two 2-mm-thick resistive High-Pressure Laminate (HPL) plates separated by a 2-mm-thick gas gap. The outer surface of the HPL plates is coated with a thin conductive graphite layer, and a voltage is applied. The RPCs are operated with a 3-component, non-flammable gas mixture consisting of 95.2% freon ($C_2H_2F_4$, known as R134a), 4.5% isobutane ($i\text{-}C_4H_{10}$), and 0.3% sulphur hexafluoride (SF_6) with a relative humidity of 40% - 50%. Readout strips are aligned in η between the 2 gas gaps. Signals coming from the strips are asynchronously sent to the Front End boards whose output is a shaped and discriminated LVDS signal.

The discriminated signals coming from the Front End boards feed via twisted cables (10-20 mt long) the Link Board System located in UXC on the balconies around the detector. The Link System consist of the 1376 Link Boards (LBs) and the 216 Control Boards (CBs), placed in 108

Link Boxes. The Link Box is a custom crate (6U high) with 20 slots (for two CBs and eighteen LBs). The Link Box contains custom backplane to which the cables from the chambers are connected, as well as the cables providing the LBs and CBs power supply and the cables for the RPC FEBs control with use of the I2C protocol (trough the CB). The backplane itself contains only connectors (and no any other electronic devices).

The Link Board has 96 input channels (one channel corresponds to one RPC strip). The input signals are the $\sim$100ns binary pulses which are synchronous to the RPC hits, but not to the LHC clock (which drives the entire CMS electronics). Thus the first step of the FEB signals processing is synchronization, i.e. assignment of the signals to the BXes (25ns periods). Then the data are compressed with a simple zero-suppressing algorithm (the input channels are grouped into 8 bit partitions, only the partitions with at least one nonzero bit are selected for each BX). Next, the non-empty partitions are time-multiplexed i.e. if there are more than one such partition in a given BX, they are sent one-by-one in consecutive BXes. The data from 3 neighbouring LBs are concentrated by the middle LB which contains the optical transmitter for sending them to the USC over a fiber at 1.6 Gbps.

The Control Boards provide the communication of the control software with the LBs via the FEC/CCU system. The CBs are connected into token rings, each ring consists of 12 CBs of one detector tower and a FEC mezzanine board placed on the CCS board located in the VME crate in the USC. In total, there are 18 rings in the entire Link System. The CBs also perform automatic reloading of the LB's firmware which is needed in order to avoid accumulation of the radiation induced SEUs in the LBs firmware.

Both LBs and CB are based on the Xilinx Spartan III FPGAs, the CB additionally contains radiation-tolerant (FLASH based) FPGA Actel ProAsicPlus.

The High Voltage power system is located in USC, not exposed to radiation and easily accessible for any reparation. A single HV channel powers 2 RPC chambers both in the barrel and endcap regions. The Low Voltage boards are located in UXC on the balconies and provide the voltage to the front end electronics.

0.3 Resistive Plate Chambers Longevity

0.3.1 Expected rates and integrated charge in the present system

The upgrade from LHC to HL-LHC will increase the peak luminosity from $10^{34}\ cm^{-2} \cdot s^{-1}$ to reach $7.5{\times}10^{34}\ cm^{-2} \cdot s^{-1}$, increasing in the same way the total expected background to which the RPC system will be subjected to. Composed of low energy gammas and neutrons from p-p collisions, low momentum primary and secondary muons, puch-through hadrons from calorimeters, and particles produced in the interaction of the beams with collimators, the background will mostly affect the regions of CMS that are the closest to the beam line, i.e. the RPC detectors located in the endcaps.
The 2016 data allowed to study the values of the background rate in all RPC system. In Figure 1 (left) the rate as a function of the instantaneous luminosity is shown for the top sectors of the third and fourth endcap stations, in the region where the maximum rate has been measured. Extrapolating linearly from the data up to the luminosity of $7.5{\times}10^{34}\ cm^{-2} \cdot s^{-1}$, and using a factor 1.2 to take into account the increase of energy from 7 to 8 TeV, the maximum rate per unit area at HL-LHC conditions expected is of the order of $400 Hz/cm^2$.

Figure 1 (right) shows the charge integrated in the Endcap RPC system from 2009 to 2016, for a total delivered luminosity from p-p collisions of about $75 fb^{-1}$. To the $4000 fb^{-1}$ of expected in-

tegrated luminosity, over the 10 years of HL-LHC lifetime, an integrated charge of $\sim 0.4C/cm^2$ can be estimated.
During Run-I, the RPC system provided stable operation and excellent performance and did not show any aging effects. In the past, extensive long-term tests were carried out at several gamma and neutron facilities certifying the detector performance up to values of dose, charge and fluence close to those expected after ten years of HL-LHC operation. Both full size and small prototype RPCs have been irradiated with photons up to an integrated charge of $\sim 0.05C/cm^2$ and $\sim 0.4C/cm^2$, respectively [? ?].

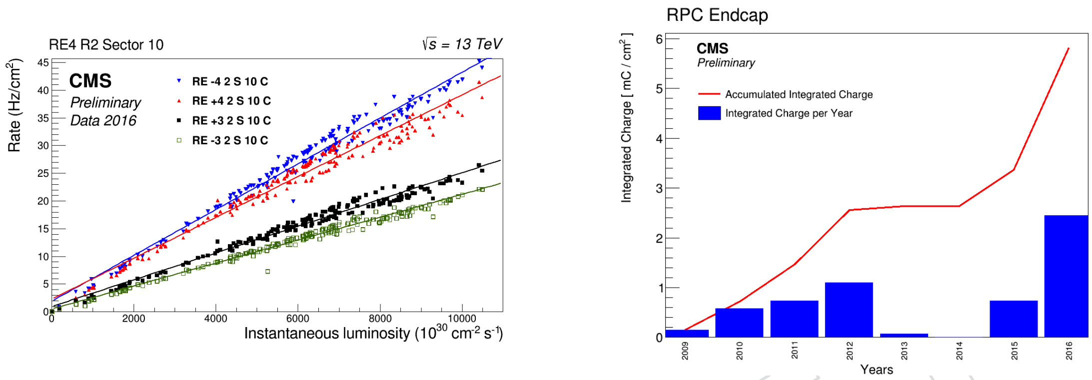

Figure 1: (left) RPC rate measured in 2016 in p-p collision runs as function of the instantaneous luminosity. Every point corresponds to a particular run. (right) integrated charge for Endcap. The integrated charge in years is shown in blue. The red curve shows the cumulative evolution of the integrated charge in time.

0.3.2 Longevity of the present system: tests and results at GIF++

In this perspective, studying the performance of the present system up to an integrated charge of $\sim 1.2C/cm^2$, 3 times higher than what expected for 10 years of operation of HL-LHC, and background hit rates of $1200Hz/cm^2$, 3 times stronger than what expected from the designed peak luminosity, and identifying possible long-term aging effects are necessary steps to take to insure that the RPCs will be able to cope with the high radiation conditions.
This study implies a monitoring of the performance of the detectors probed using a high intensity muon beam in a irradiated environment by periodically measuring their rate capability, the dark current running through them and the bulk resistivity of the Bakelite composing their electrodes. GIF++, with its very intense ^{137}Cs source, provides the perfect environment to perform such kind of tests.
As the maximum background is located in the endcap region, the choice naturally was made to focus the GIF++ longevity studies on endcap chambers. The RPC chambers for both Barrel and Endcap regions have been built in the period 2005-2007, except the chambers for the fourth endcap (RE4/2 and RE4/3) stations that have been built in 2013-14 and installed during LS1. For this reason, fours spare chambers two RE2/2 (old production) and two RE4/2 spares (new production) have been selected for this aging test. Having two chambers of each type allows to always keep one of them non irradiated as reference, the performance evolution of the irradiated chamber being then compared through time to the performance of the non irradiated one. The performance of the detectors under different level of irradiation is measured periodically during dedicated test beam periods using the H4 muon beam. In between these test beam periods, the two RE2,3/2 and RE4/2 chambers selected for this study are irradiated by the ^{137}Cs

source in order to accumulate charge and the gamma background is monitored, as well as the currents. The two remaining chambers are kept non-irradiated as reference detectors.

Figure 2 shows the maximum efficiency for the RE2 and RE4 chambers (for both irradiated and non irradiated chambers) as a function of the background rate in two different test beam periods. The method for the data analysis is described here [?]. No aging has been observed so far.

Figure 3 shows the maximum efficiency for the RE2 and RE4 chambers as a function of the integrated charge as measured with the muon beam with a background hit rate of $300 Hz/cm^2$, almost equal to the expected HL-LHC conditions. In order to spot possible aging effects coming from an increasing integrated charge over the time, detector performance of exposed and not exposed chambers are compared in the plots.

To complete the aging study, the Bakelite resistivity is regularly measured by fluxing the chamber with Argon and performing an HV scans. In Figure 5 the RE2 and RE4 resistivity as a function of the integrated charge is showed. Finally the noise rate is monitored weekly during irradiation periods (Figure 6). No signs of aging were observed and further investigation is needed to get closer to the final integrated charge requirements proposed for the longevity study of the present CMS RPC sub-system.

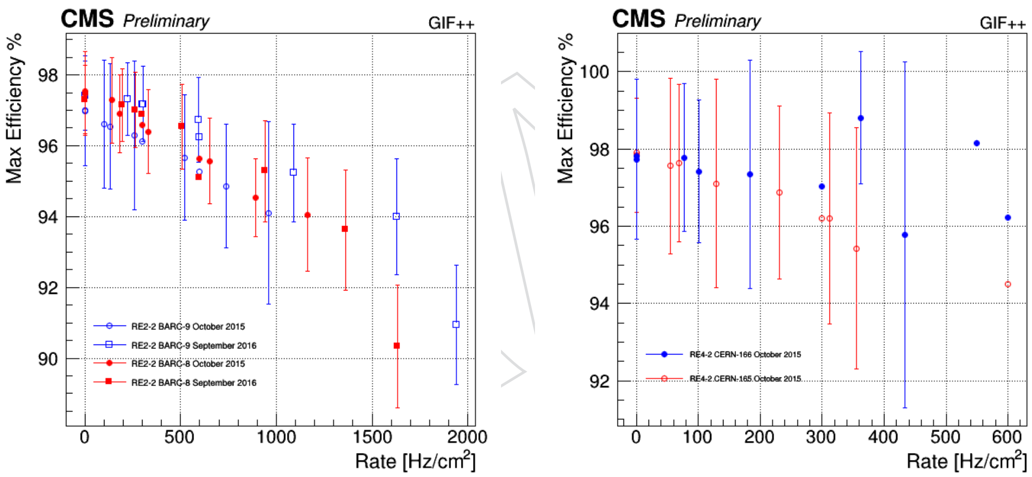

Figure 2: Evolution of the maximum efficiency for RE2 (left) and RE4 (right) chambers with increasing extrapolated γ rate per unit area at working point. Both irradiated (blue) and non irradiated (red) chambers are shown.

0.3.3 Front-end board longevity

The RPC on-detector electronics consists of LV distribution boards, which distribute LV power and slow-control signals, and front-end boards (FEBs,) which amplify and discriminate the signals induced on the strips and transmit them to the RPC Link Board system located in the CMS tower racks.

During Run-I, very few failures or malfunctioning of FEBs (23 over 6016) have been reported. The FEBs had been previously tested up to a neutron fluence of about 10^{12} n/cm^2 and no

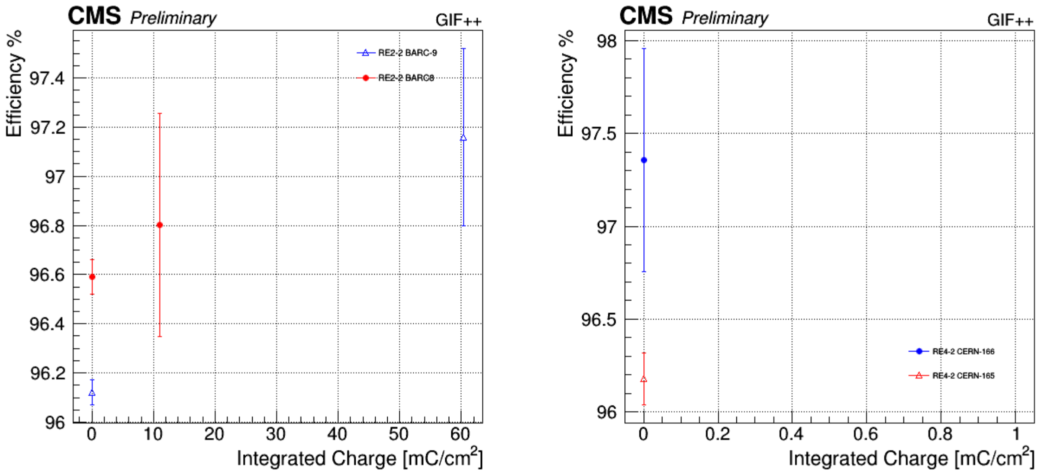

Figure 3: Evolution of the maximum efficiency at HL-LHC conditions, i.e. a background hit rate per unit area of $300 Hz/cm^2$, with increasing integrated charge for RE2 (left) and RE4 (right) detectors. Both irradiated (blue) and non irradiated (red) chambers are shown. The integrated charge for non irradiated detectors is recorded during test beam periods and stays small with respect to the charge accumulated in irradiated chambers.

Figure 4: Comparison of the efficiency sigmoid before (triangles) and after (circles) irradiation for RE2 (left) and RE4 (right) detectors. Both irradiated (blue) and non irradiated (red) chambers are shown.

damage was observed [?]. In order to qualify the FEB performance at the higher doses and fluence, a new campaign of neutron irradiation testing is planned. Since the FEB electronics is basically analog, SEUs would negligibly increase the spurious noise rate. In addition, by the end of Run-I, about 1% of RPC electronic channels were masked due to a failure in the distribution board caused by discharges in the chamber. A new generation of distribution boards, with stronger protection against discharge, has been already produced and 23 out of 360 barrel distribution boards have been replaced during LS1.

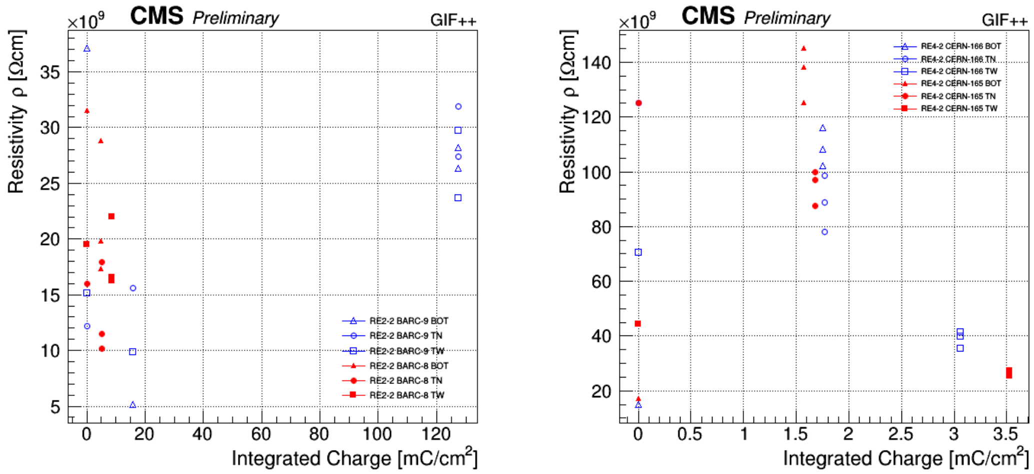

Figure 5: Evolution of the Bakelite resistivity for RE2 (left) and RE4 (right) detectors. Both irradiated (blue) and non irradiated (red) chambers are shown.

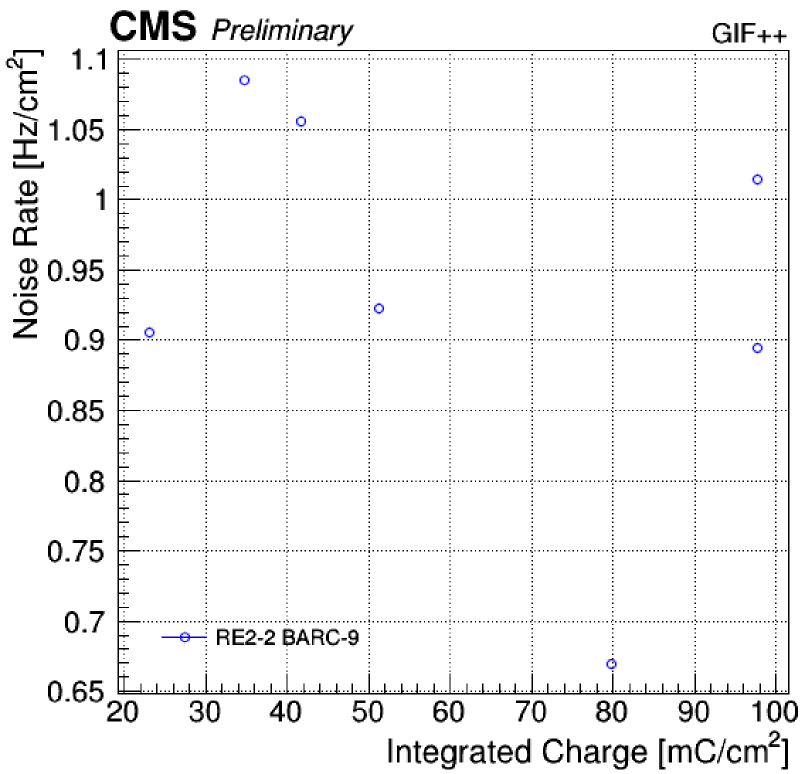

Figure 6: Evolution of the noise rate per unit area for the irradiated chamber RE2-2-BARC-9 only.

0.3.4 Limitations of the RPC Link System

The RPC Link System receives the data from the detector FEB via the copper cables in the LVDS format, then synchronizes them, compresses and sends them via the optical links to trigger processors (TwinMux, OMTF and CPPF). Both LBs and CB are based on the Xilinx Spartan III FPGAs, the CB additionally contains radiation-tolerant (FLASH based) FPGA Actel ProAsicPlus. The Link System components were produced between 2006 and 2007. It is a custom electronics containing many different devices. High-Temperature Operating Life (HTOL) has been performed by the Xilinx company in order to estimate the failure rate of the FPGA devices. From these tests, few FPGA chips failures can be expected during 20 years of operation of the RPC link system (it contains in total 2860 Spartan III FPGAs). For other devices used on the LBs and CBs (FLASH memories, TTCrx, GOL, CCU25, QPPL ASICs) such estimations are not available. [to be mentioned the spares sistuation]. The ionising radiation levels on the detector balconies is relatively low, therefore it was used on the LBs and CBs the SRAM based FPGAs which are vulnerable for the Single Event Upsets (SEUs). In run 2, to avoid accumulation of the radiation induced SEUs the firmware is reloaded periodically (every 10-30 min). These methods work well; we have not observed any significant impact of the SEU on the system performance. During the LHC operation the SEU-like problem is detected by the online software with frequency of one error per a few days (for the full system).

The CBs are connected into FEC token rings, therefore if one CB fails then the entire ring does not work, leading to a loss of a significant part (1/18) of the system. Moreover, the identification of the malfunctioning board is difficult and time consuming, preventing prompt repairation during any short break of the LHC operation. The CBs are connected into the token rings with copper Ethernet cables, some of them are over 10 m [FIXME] long. Therefore, the ring operation can be disturbed by the electromagnetic noise which results in the errors during the software read or write operations. The impact of this problem was minimise by a modification of the CB hardware and firmware. Additionally, in the control software the methods for autorecovery after the errors in the ring operation were implemented. As a result, the CCU errors are relatively rare now, however still sometimes results in a problem with the configuration of the Link System for the running. The above problems lead only a few time to a loss of the beam time during the LHC operation between 2010 and 2016. However, it is possible that with the aging of the electronics they may become more frequent.

0.3.5 The quest for eco-gas

For applications where high background rates are expected, RPCs have to be operated in avalanche mode in order to keep the total produced charge low with benefits in terms of aging and rate capability. This is usually obtained with suitable gas mixtures that prevents the transition from avalanche to streamer modes keeping the detection efficiency above 90%. The use of Fluorine (F)-based gases, usually used in refrigerants, has shown so far to give the best performance. As already outlined in section 2.1.2 (?) recent European regulations demand the use of environmentally un-friendly F-based gases to be limited or banned. In CMS, RPCs are operated with a gas mixture of $C_2H_2F_4$ (R134a) 95.2%, isobuthane 4.5% and SF_6 0.3% for a the total GWP 1430 mainly drived by the R134a.

In the last years a program of measurements has been started inside the CMS Collaboration in order to find the right eco-friendly candidate given the constrains defined by the front end electronic used in the CMS experiment. The present CMS front-end electronics use a discriminator threshold corresponding to about 150 fC, lowering this value would increase the electronic noise at unacceptable levels. At the same time we would try to work with an operation Voltage no much more than 10 kV as the CMS power supply system (including cables and connectors) has been certified up to 12 KV and we would like to mantain a safety margin of about 20 %. An overview of potential gas candidates can be found in [ref].

0.3.5.1 search for eco-friendly gas mixtures for RPC operations

A big R&D effort has started in Frascati and Ghent Laboratories also in collaboration with ATLAS groups to find a valid replacement for the $C_2H_2F_4$. In parallel is under study also the possibility to recover the exhaust of the gas after the circulation in the detector in order to not pollute the atmosphere.

The Laboratory set-up in both Frascati and Ghent are explained in [ref rpc2016]. Two main components have been identified as possible substitute of the $C_2H_2F_4$ that is the main contributor on the GWP of the RPC system: Thetrafluoroporpane ($C_3H_2F_4$) and CF_3I. Both components have a big impact on the reduction of the avalanche charge and move the working point to voltage values above the RPC power system limits. So the approach has been to add fraction of CO_2 to the gas mixture in order to be able to work at lower HV values. The drawback is that the streamer probability increase with bad effects on the rate capability and the aging of the detector. So a fine tuning of each gas component is fudamental to reach the right gas mxiture.

As a backup solution, gas mixtures where $C_2H_2F_4$ is still present, but with much lower percentage have to be considered.

In fig. 7 (left) a complex gas mxiture with five components: 26 % of $C_2H_2F_4$, 24.7 % of $C_3H_2F_4$, 44 % of CO_2, 4.8 % of iC_4H_{10}, 0.5 % of SF_6 for a total GWP=493 has been tested. The results in terms of efficiency and stremaer probability are more than satisfactory with a working voltage just few hunderd volts above the safety margin defined for our system. The GWP is about one third with respect to the present CMS gas mixture. Further tests fine-tuning the gas component fractions are in progress with the goal to find the best option.

Very interesting results have been produced with CF_3I of CO_2 gas mixtures as shown in fig. 7 (right) Here the working point is below 10 kV as desired and efficiencies above 90 % are obtained with streamer probabilities around 10 %.

In this case the drawback is the high price of the CF_3I that has to be taken into account. More details can be found in [ref].

Additional crucial tests to evaluate also the cluster size have been planned and will be performed before the end of the year. The R&D program is ongoing with the plan to define the best two gas mixtures to be tested at GIF++ by the end of 2017. It has to be considered that in all the tested mixtures the total charge generated is larger than that generated by the standard CMS RPC gas mixture and that the plateau region streamer free is much reduced. Careful validation of the RPC performance has to be carried out at GIF++ to study the aging and the rate capability.

The quest for a suitable eco-friendly replacement is a multi-parameter problem which has to take into account several issues, i.e., physics performances, flammability/toxicity/handling hazards, matching with available electronics and, last but not least, compatibility with the materials used in muon detectors. So in parallel to detector performance studies, the materials compatibility is subject of studies performed in INFN Frascati and Sapienza Università di Roma, faculty of Engineering, making use of microanalysis apparata such as chemistry lab, gascromatograph-mass spectrometer, scanning electron microscope - EDS, x-ray diffractrometry, Fourier Transform Infra Red Spectroscopy (FTIR), etc.

The properties of materials used in RPC detectors are compared (by means of SEM-EDS, XPS, XRD, FTIR analyses) before and after exposure to candidate ecogases in standard operating conditions. To expedite the ageing process, materials samples are exposed to candidate gases in a pressurised detector (fig.8 left). Preliminary results for RPC bakelite samples exposed in

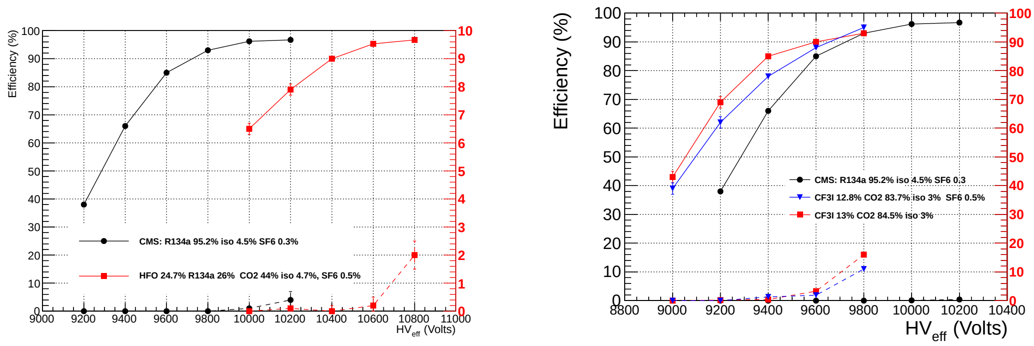

Figure 7: Efficiency (solid line) and streamer probability (dashed line) as a function of the effective working voltage for: Five components mixture based on $C_3H_2F_4$, R134a, CO_2, iso-buthane and SF$_6$ (left), CF_3I, CO_2, iso-buthane and SF$_6$ (right). Mixtures are compared with the present RPC CMS gas mixture.

HFO-1234ze atmosphere at 2 bar for 4 months show no difference in FTIR spectra with respect to unused samples (fig.8 right).

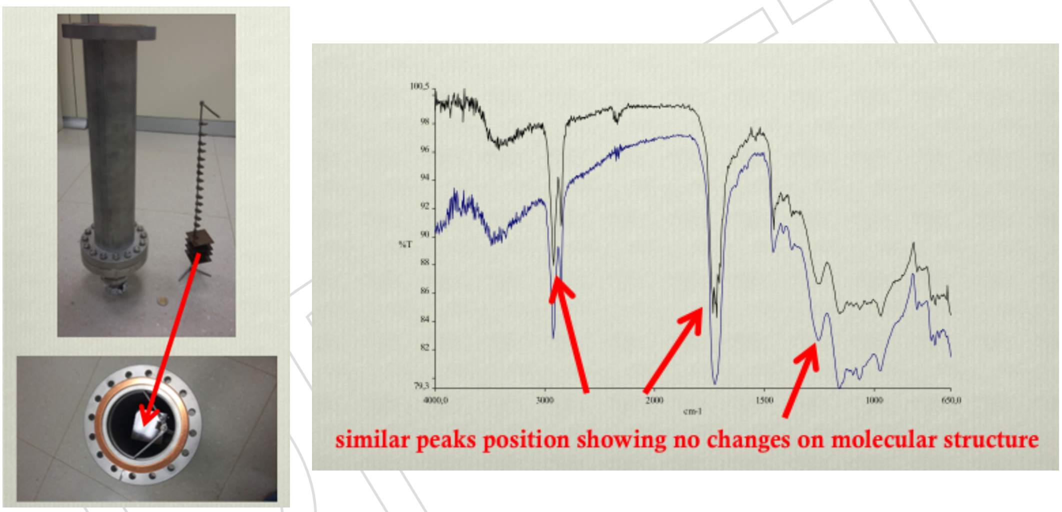

Figure 8: Left: Reactor used to test the RPC materials exposed to HFO-1234ze component. Right: FITR spectra comparing exposed and not exposed saples after a period of 4 month. No evidence of difference in the molecular structure

0.3.5.2 Alternative options

If suitable eco-friendly gases are not found, the following steps are planned:

- Install a commercial abatement system to "burn off" the RPC exhaust gas. These units are commonly used in the semiconductor industry and several manifacturers are available.
- The previews step will be effective only if all the RPC gas flow thorough the exhaust where it can be burned off. Currently RPC system leaks about 1100 liters per hour due to 47 leaking chambers around the barrel system. The plan is to reduce these leaks below 50 l/hour ... plans on how to do

- Add a recuperation system for RPC gases. Once the largest fraction of the gas go thorough the exhaust it can be easly recovered .... .

0.4 Upgrade of the RPC Link Board System

0.4.1 Motivations for a new Link Board System and use of RPC timing

As reported in section 0.3.4 the present Link Board system could not perform with the same efficiency in the long term. A new system is needed to improve the robustness of the RPC readout and the possibility to upgrade and maintain the firmware. In addition to the overcome of the hardware limits, the new LB system will be upgraded in such a way to explore the full timing capabilities of the detector at trigger and reconstruction level.

As already described in the section 0.2, although the RPC detectors have an intrinsic time resolution [cite paper] of the order of 1 ns, the link board system based DAQ system of the RPCs during phase 1 records the RPC hits informations at step of one BX (25 ns) loosing the full timing power of the detctor.

The link board upgrade proposed for phase 2 will overcome this limit enhancing the performance of the system from the timing point of view. The higher background expected in the phase 2 LHC operations will be strongly mitigated by the precise timing tag of the RPC, cleaning the hits to complement the DT and CSC informations in muon offline recosntruction and triggering. During phase 2 the muon trigger system will be reviewd and a possible approach is to analyze all the hits coming from DT, CSC and RPC in a global way in the new back-end of the muon trigger. The information of a precise timing from the RPC hits will be available at trigger level very soon and can be used to reject out-of-time muons and background hits. Moreover the timing informations coming from the muon system have a key role in the HSCP analysis (see section on physics and trigger: camilo+Luigi). During phase 1 DTs and CSCs timing have been used at offline level together with the RPC information with BX granularity to identify slowly moving stable charged particles. No dedicated trigger using timing informations is available. In phase 2 the fast and precise timing from the RPCs can be available at trigger level and can be used to define a HSCP dedicated trigger implementing a coherent out-of-time coincidence of hits in the RPC stations. Moreover at offline level the RPC timing will complement with similar and in same case higher time resolution the DT and CSC informations improving the search strategy and mass measurement of thses particles [see camilo+Luigi part].

0.4.2 The new Link Board System

Based on previous explanations about link board (LB) and control board (CB) limitations, the performance of some components such as CCU and TTCrx chips are not efficient. In addition, CCU, TTCrx GOL and QPLL ASICs are not available now. Since, redesign of these ASICs are time consuming and overpriced, so suitable alternatives must be found. One of the best ways to overcome the present limitations is implementation of these chips by FPGAs. Since FPGAs are truly parallel in nature so different processing operations do not have to compete for the same resources and each independent processing task is assigned to a dedicated section of the chip and can function autonomously without any influence from other logic blocks. Therefore for true parallel coincidence execution between the signals from many RPC detectors with the LHC clock, FPGA is the best candidate. In addition, FPGA chips can keep up with future modifications that might be necessary. As a product or system matures, the performance of the link board can be improved without spending time for redesigning hardware or modifying the board layout, which is a grate feature for future upgrades of Muon system. Although, implementation and optimization of four important chips of LB and CB by FPGA is a new challenge, the design, implementation and testing of TTCrx core already done by INFN group for the RE4 development, shows that this approach can be satisfactory and considering in addition the possibilty to correct for SEUs, that was not included in the previews implementation.

0.4.2.1 Radiation effects on commercial FPGAs

Most Commercial chips can be safely used for Total Ionization Dose (TID) of few krad. Since the TID on place of LB for 10 years work of LHC with nominal luminosity, is below 100 rad, the TID is not a problem and there is no need to use radiation hardened electronics. Therefore, the GOL chip and other radiation hardened chips which can be safely used even for TID in order of Mrad are overqualified for the LB system. But, the most important radiation effects i.e., SEU on RAM-based or FLASH based commercial FPGAs must be corrected. The experimental results on the FPGA-GTX show that the SEUs only cause rare transient bit errors in the data and no mitigation is needed. But, for Configurable Logic Block (CLB) and Block RAM (BRAM) of new family of FPGAs, the effect of SEU is more complicated.

In new FPGA families, the transistor size has dramatically decreased, enabling more congura-tion logic cells to be packed into the same amount of physical area due to the smaller process technology of each family. The amount of area aected by one radiation particle strike has not changed, but the number of logic cells and transistors inside that area has increased. In addition, the smaller transistors have lower threshold which make it easier for the logical value stored in the SRAM cell to experience an upset. So, performing the error correction techniques on one of important building blocks of new FPGA families i.e., CLB is more critical. The SEU typically affect a single bit in a single cell of FPGA BRAM, which can be mitigated by error detection and correction methods. The calculations based on experimental results show that without considering the chip cores which are implemented by FPGA, by using Vertex 6 instead of Spartan III in LB and CB, the SEU in CLB will be around five times greater. So, GOL, CCU, QPLL and TTCrx cores must be implemented by suitable commercial FPGAs through some reliable SEU mitigation capabilities in comparison to present LB system.

0.4.2.2 SEU Mitigation in FPGA

Since all the ASIC chips of the LB and CB must be implemented by FPGA, applying suitable SEU mitigation methods for different FPGA areas are more critical. All SRAM or FLASH based FPGAs, contain SRAM blocks and flip-flops (FF) which are susceptible to SEUs. The SRAM cells have a very high susceptibility to SEUs. So, the FPGAs using SRAM cells for device configuration will need special mitigation techniques in order to prevent loss of functionality when struck by a heavy ion. The FFs which are the most robust of memory structures are only upset in high-radiation environments.

There are several methods for SEU correction such as Error Correction Code (ECC), Cyclic Redundancy Check (CRC), Blind Scrubbing, Read back Scrubbing, Conguration Scrubbing (CS), Memory Scrubbing and Triple Module Redundancy (TMR). If the upset occurs in data SRAM, error detection and correction (EDAC) techniques can be used to mitigate the error. The ECC is a redundancy coding mechanism that is useful for correcting Single Bit Upsets (SBU). CRC is particularly useful for detecting Multi Bit Upsets (MBU) across an FPGA. Although, any multi-bit error requires the device reconfiguration, but since in the new families of Microsemi FPGAs, SRAM bits in each logical word are physically separated, the probability of the MBU resulting in uncorrectable errors is dramatically reduced. The built-in ECC feature in FPGAs can be used to protect data integrity and prevents software controlled write and read process for BRAM memory tests. The experimental results for FPGA Vertex 6 show that even by using the simple

ECC method, the SEU Mitigation strategy completely works and no errors are detected in the BRAM contents.

If the error occurs in the SRAM configuration memory used to control the personality of an SRAM-based FPGA, a logic failure or firm error of the FPGA may result. In this case, the simple blind scrubbing strategy which is used in current LB, continuously overwrite to the conguration memory from a protected golden le. Although, this method has fast correction speeds, but inherently is unable to detect upsets. Moreover, inefficiently a signicant portion of processing bandwidth is wasted continuously for reconfiguration of unaffected FPGAs configuration memory. This problem can be solved by Flash-based FPGAs or CS technique in SRAM-based FPGAs. In CS method, the memory is checked periodically, the upsets are detected and the dynamic partial reconguration is used to overwrite the upsets. The initial conguration must rst be completed before any scrubbing can occur. The CS method is usually performed at periodic intervals while the FPGA is in operation (dynamic reconguration). This partial reconguration is not intended to interrupt normal FPGA operation.

The TMR in SRAM-based FPGAs are used for SEU in logic and FFs and for the Flash-based FPGAs it is only used for SEU correction in FFs. In a design with TMR method, the design circuitry is triplicated into three identical copies and typically placed at three dierent locations in the FPGA. Such solution provides protection against SEU in the registers, however it does not provide protection against radiation generated glitches in the combinatorial logic. To avoid a single point of failure in the voter circuit, the voters are often triplicated as well. However such solution would consume too much resources of FPGA. When an upset occurs in one of the TMR modules, the error needs to be repaired quickly before another upset aects a second module, causing TMR to fail. It is worth noting that just having a repair mechanism (like scrubbing) without TMR would fail instantly if the ionizing radiation were to upset a sensitive bit and cause the circuit to malfunction. Thus, both TMR and scrubbing are necessary to achieve an overall reliability improvement of LB and CB system. It must be noted that SEU correction methods usually need complex operations which cant be performed in a clock cycle. Because of this latency, the SEU mitigation methods in the CB system must be performed with much more care.

0.4.2.3 Some improvements and upgrades in LB and CB

0.5 Extension of the RPC system

0.5.1 Motivations

With the LHC luminosity expected in phase 2, the in-time pileup will be right at the edge of the CMS design envelope and will present special challenges for the muon system to trigger on high-pT muons. The RPC upgrade is essentially driven by the impact of the instantaneous peak luminosity on the trigger system. In the endcaps, the RPC system provides excellent timing with a somewhat worse momentum resolution compared to the CSC system. To be effective, the muon trigger must achieve good enough resolution to identify high-pT tracks. The problem stems from mis-measurements of low-pT muons, that are promoted to high-pT muons and contribute to the trigger rate. With the much higher flux of low-momentum muons at increased luminosity, the use of additional informations in stations 3 and 4 will help to remove the CSC ambiguities in case of events with more muons crossing the same CSC chamber and to keep under control poorly measured muons.

CSC system provide high efficiency for identification and triggering of muons in the endcap region. Neverthless as can be seen in figure 9 there are gaps between CSC chambers where the identification and the trigger performance are lower because of the reduced number of segments available.

Hits coming from RPC stations add the needed redundancy in such regions providing appropriate spatial resolution to correctly contribute to the P_t assignment. Impact of RPC hits in the lower η endcap region, already covered by these detectors, on the single muon trigger efficiency can be seen on figure 9 [this figure should be checked with CSCs].

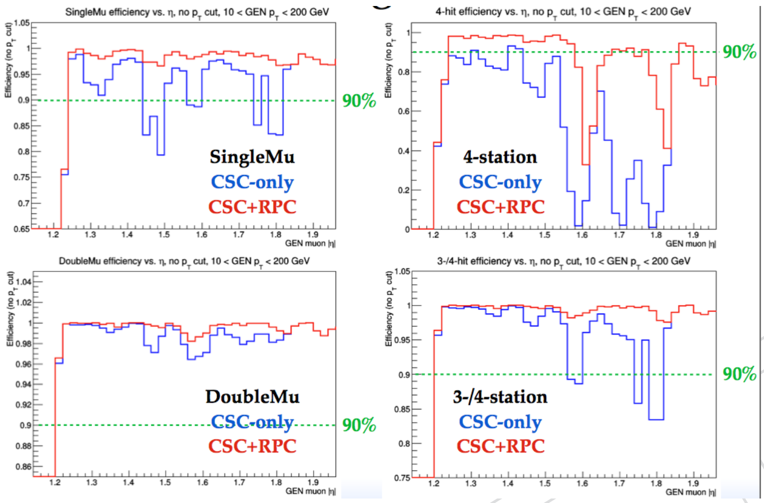

Figure 9: Impact of RPC hit inclusion on the muon trigger performance during phase 1 in the lower region of the endcap system.

The plot in Fig. 10 shows that at 140 PU, even for a perfectly working existing system (red curves), the typical stub reconstruction efficiency drops below 90% with significant dips due to the high-voltage spacers inside the CSCs. The reduction in the average number of reconstructed stubs on a track in turn increases the frequency of muon pT mismeasurements, which inflates the trigger rate and flattens the rate curve. The same figure shows that the installation of RE3/1 station (the RE4/1 case is very similar to RE3/1) restores the local-reconstruction (stub) efficiency.

The extentsion of the RPC system in stations RE3/1 and RE4/1 will provide the additional hits to recover these inefficiency patterns at the station level, with benefits for the efficiency and robustness of the trigger performance (need a figure showing the impact on trigger objects, work in progress).

RPC Informations will be also useful to remove the CSC ambiguity in cases where two or more muons cross the same CSC chamber. The plan for the RE3/1 and RE4/1 envisage a 2D strip readout measuring the arrival time of the RPC signal on both ends of the strip and recovering the position along the strip looking at the time difference [see section elctronics and layout]. With such method a resolution of the order of few cm is expected so that the CSC ambiguity can be removed directly at station level.

The advantages already described in having an improved timing of the RPC system will be extended in this region with the RE3/1 and RE4/1 installation.

In HSCP searches between 11 and 14 % of the events are in the region covered by the RPC extension (put figure). A dedicate HSCP trigger based on RPC hits will extend the discovery reach in this region [ref camilo section].

0.5.2 Overview of the requirements and technological choices

The two new stations of RPCs, RE3/1 and RE4/1, will be installed in muon disk 3 and 4 respectively, covering the $1.8 < |\eta| < 2.4$ region and complementing the already existing CSCs in that range in stations ME3/1 and ME4/1.

The overall design of the new stations is relatively similar to the existing RPC endcap stations, with wedge shaped detectors, each spanning 20° in φ with radially oriented readout strips. This means the full project consists of adding 18 new chambers per muon disk, i.e. 72 chambers in total for the RE3/1-RE4/1 stations in both endcaps. Each station will provide one single hit for muon reconstruction.

FIXME - Detector envelopes: RE3/1 (ΔR = 1776 mm between $R = 1526 - 3302$ mm); RE4/1 (ΔR = 1581 mm between $R = 1709 - 3290$ mm); add also the space available in Z - I suggest adding a technical drawing of the chambers as in Fig. 11.

FIXME - Check these numbers and update

According to FLUKA simulations and by a comparison with CSC chambers already located in the region where RE3/1 and RE4/1 chambers will be mounted, a rate of about 2kHz/cm^2 (including a safety factor of 3) is expected in the hottest points of these new RPC stations (figure 12).

FIXME - Add expected rate plots from Alfredo for RPCs, see GMM meeting, CMS Week Jan, 2017;

To sustain the expected rates and perform with efficiency above 90% also in this region an improved version of the RPCs (*i*RPCs) has been developed.

The rate capability can be imporved in various ways:

- Reducing the elctrode resistivity and/or thickness, wich has the effect of reducing the recovery time needed for the electrodes to be charged up again after a discharge

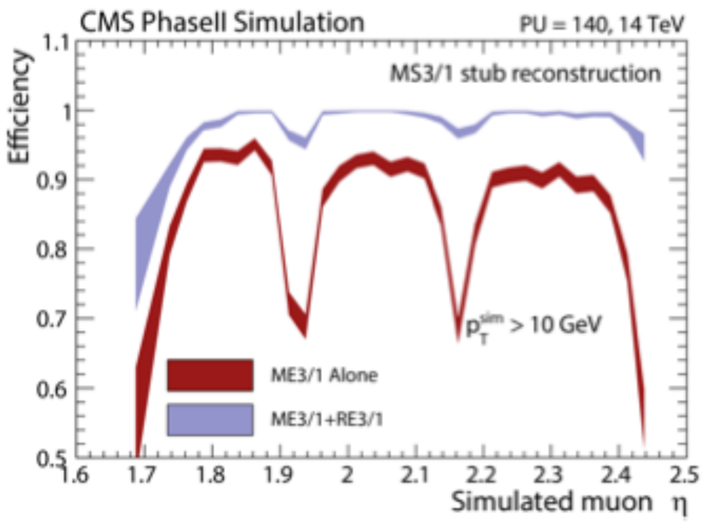

Figure 10: The Local-trigger efficiency ("stub") in station 3 as a function of eta, for the present Phase-1 detector and with the addition of RE3/1 chambers.

in the gas gap.

- Reducing the average charge generated in the avalanches, and transferring part of the signal amplification from the gas to the front-end electronics. Reducing the overall charge path in the gap indeed results in a reduced voltage drop on the electrode plates, and a reduced period of inefficiency; this also reduces the aging process.
- Changing the detector configuration, which includes different number of gaps, different gas and electrode thickness, that could enhance the performance of the detector.

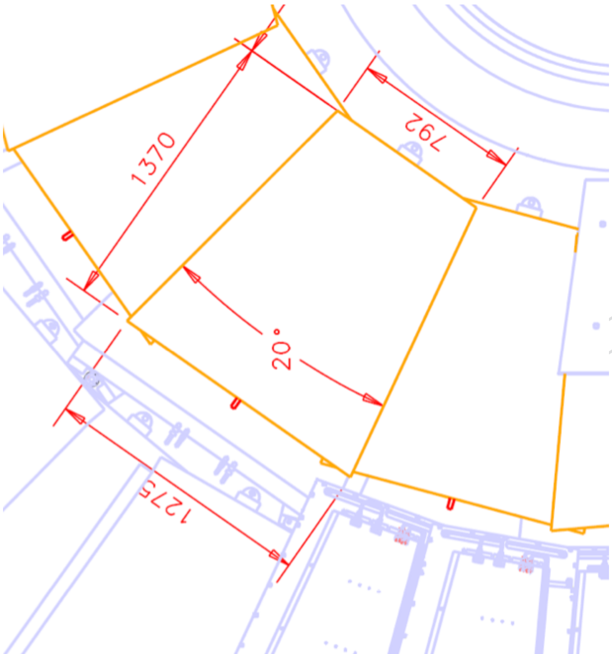

Figure 11: Detector envelope for the RE4/1 chambers.

rpc/figures/rateExpectedHighEta.pdf

Figure 12: Expected rate for HLC Luminosity of xxx in the region covered by RE3/1.

In addition, aging effects during the full HL-LHC program need to be accurately considered, as discussed in the section 5.x.x for existing detectors. For an expected rate of 2 kHz/cm^{-2} and an average charge per avalanche of 20 pC, the integrated charge in the detector after the integrated luminosity of 3000 fb^{-1} will reach about 2 C/cm^2 (including always a safety factor of 3). Tests at GIF++ have been planned in order to integrate the full charge during the second part of 2017 and 2018.

From the readout point of view as reported in the section [rpc upgrade motivations] we need to provide RPC hits with a time resolution of the order of 1 ns and a spatial resolution of the order of few mm in the phi direction. In addition a resolution of few cm in the η direction will help to remove CSCs ambiguities when more muons cross the same chamber.

0.5.3 Baseline option: Double gap RPCs

To satisfy the requirements mentioned in the previous section, as baseline option we adopt a lower-gain avalanche-mode operation to achieve a higher rate capability of far exceeding 2 kHz cm^2 as well as to ensure the longevity of the RPC gaps[**?**].

As in the case of the present system a double gap readout with pick-up strips in the middle is considered.

To reduce the detector aging and to improve the rate capability both the electrode and gas gap thickness are reduced and part of the amplification is moved to an improved front-end electronic [ref. electronic chapter].

Improving sensitivity of pulse-digitization electronics is the major factor to enhance both detector rate capability and longevity for the CMS RPCs. In addition reducting the electrode thickness and keeping its resistivity in the range $0.9 \div 3.0 \times 10^{10}$ ohm cm^{-1} reduce the recovery time of the electrodes and imporve the rate capability.

In the present baseline design for the *i*RPCs, a thickness of 1.2 (or 1.4 mm) for both gaps and electrodes is chosen instead of the 2 mm used for the current CMS double-gap RPCs.

We systematically examined the pickup charges of the avalanche pulses drawn in six double-gap RPCs constructed with gap thicknesses ranging between 1.0 and 2.0 mm [**?**]. Figure 13 shows the pickup charges drawn in the 1.2- (squares), 1.4- (triangles), 1.6- (open circles), and 2.0-mm (full circles) double-gap RPCs as a function of the electric-field intensities whose values were converted to the effective ones under the standard conditions of P = 1013 hPa and T = 293 K. The tetrafluoroethane-based gas mixture for the standard CMS RPC operation (95.2% $C_2H_2F_4$, 4.5% i-C_4H_{10}, and 0.3% SF_6) was used for the data.

Figure 13 clearly menifests that the thinner gap thicknesses more effectively retard the fast growth of the pickup charges of the ionization avalanches even in the low electric field regions. This implies that the use of the thinner gaps will effectively preserve the size of the operational plateau when we lower the digitization threshold to enhance the detection sensitivity. The reduction of the operational high voltage as the result of decreasing the gap thickness and the digitization threshold will be also fairly conducive to mitigating the probability of high-voltage failures, *i.e.*, to improving the electrical safety of the detectors.

The electrode resistivity is maintained in the range from 0.9 to 3.0×10^{10} Ω cm and can be achieved with high pressurized larminated (HPL, Bakelite) as for the present RPC CMS system. Working prototypes have been also produced with low resistivity glass (10^{10} $\Omega \cdot$ cm) [reference to GRPC] that due to its stiffness can be realized with plates as thin as 0.7 mm. This makes glass electrode very attractive with the possibility of having very thin gaps and thus a reduced avalanche charge. Tests have shown good performance [reference to GRPC], however the limited size of this kind of glass ($30 \cdot 32\ cm^2$) does not allow the realization of large RPC detector in a simple way, so this material will be considered only as backup solution for the HPL baseline option in case the longevity tests in progress and that will continue also after the tdr publication will show aging effects for the HPL RPC configuration.

Resistivity values lower than the range explored make the detector behaviour instable and have not been considered for the RPC upgrade program.

The pick-up strips are placed in the middle between the two RPC gaps and are embedded in a readout board made of two parts; a large trapezoidal Printed Circuit Board (PCB) and a mezzanine. The PCB hosts 192 strips with a pitch of 6 mm at the lowest eta position of the chamber, up to about 3.75 mm at the highest one. The strips are separated from the anode of each of the two gaps thanks to a dielectric layer. The thickness of the dielectric layer and its relative permittivity determine the final impedance of the strips using the HV ground planes placed on the detectors anodes as a reference. Both ends of each strip are connected to two different channels of the front end electronics RPCROC ASIC [ref section on electronics]. The ASICs as well as the TDCs are hosted on the mezzanine that is fixed on the cassette (Fig. 14). To connect a strips end to an ASIC channel a coaxial cable with the same strip impedance is used. It is soldered on one side to the strips end and on the other side to a termination board to be plugged on the mezzanine. This board hosts for each of the connected cable a dedicated circuit to match the ASIC input entry of about 200 Ω. In addition to the 6×64 channels RPCROCs, the mezzanine has the same number of TDC channels (384). The TDCs will run either on an FPGA or on a dedicated chip. On the same mezzanine an LpGBT chip is ensuring the communication between the RPCROCs and the TDCs on the one hand and a dedicated back-end RPC DAQ board on the other hand. The two boards are connected by an optical link.

0.5.3.1 RPCs Performance tests and aging studies

Two batches of HPL manufactured at Puricelli in 2015 and 2016 have been used for constructions of thin double-gap RPCs prototypes at Korea Detector Laboratory (KODEL). The quality of the new HPL of Puricelli has been proven by systematic tests of the prototype RPCs with

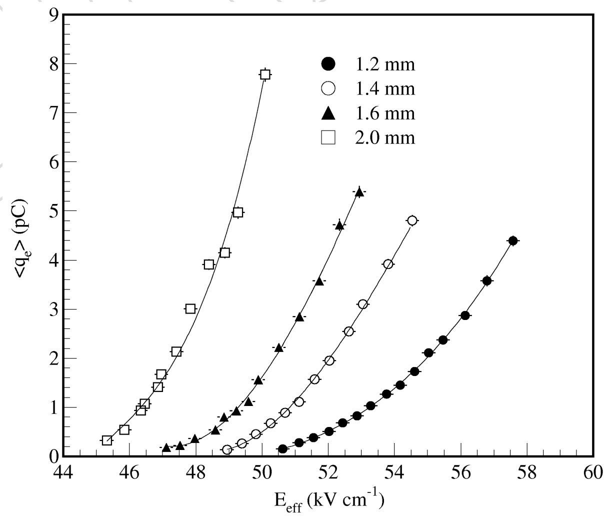

Figure 13: Mean fast charges measured on 1.2- (full circles), 1.4- (open circles), 1.6- (triangles), and 2.0-mm (squares) double-gap RPCs, as a function of the electric field intensity.

muons and gamma rays at GIF++/CERN and KODEL.

Figure 15 shows muon efficiencies (ε_μ) and mean cluster sizes in strips unit ($< C_s >$) (left), and the same muon efficiencies and probabilities of large pulses defined as $C_s > 6$ (right) as a function HV_{eff} [?], measured on the 1.2-mm double-gap RPC under a condition of no gamma background. The data measured at digitization thresholds of 250, 500, and 1,000 μV in the voltage-sensitive FEBs are labelled with the full circles, the open circles, and the squares, respectively. They are approximately equivalent to charge thresholds of 40, 80, and 160 fC, respectively, in the typical charge-senitive mode FEBs that are currently being used in the operation of the CMS RPCs.

The shift of the working point (WP) in HV_{eff} (HV_{WP}) by lowering the threshold value from 1,000 to 250 μV was measured as about 150 V (about 2.5%) in the electric field intensity. Here, we define HV_{WP} for the present 1.2-mm double-gap RPC as HV_{95} + 100 V. By estimating from the data in Figure 13, the reduction of the threshold value by the factor 4 leads to the shift of the WP in the electric field intensity by 1.28 kV cm^{-1} (154 V in HV_{eff}), and resultingly, reduces the mean pickup charge by a factor 2.5.

The prototype 1.4-mm double-gap RPC was also examined with cosmic muons but at a fixed threshold value of 300 μV. Figure 16 shows ε_μ and $< C_s >$ (left) and ε_μ and $P(C_s > 6)$ (right) as a function HV_{eff}, measured under the same condition of no gamma background. The value of HV_{WP} for the 1.4-mm double-gap RPC was defined as HV95 + 110 V.

A criterion to evaluate the rate capability of the trigger RPCs is to determine the background rate at which the shift of the WP approaches the size of the operational plateau. The detector properties related with the high-rate background were crucially examined using a 5.55-GBq ^{137}Cs source.

Figure 17 shows ε_μ and $< C_s >$ at Th = 250 (left), 500 (middle), and 1,000 μV (right) as a function of HV_{eff}, measured on the 1.2-mm double-gap RPC with (open circles) and without

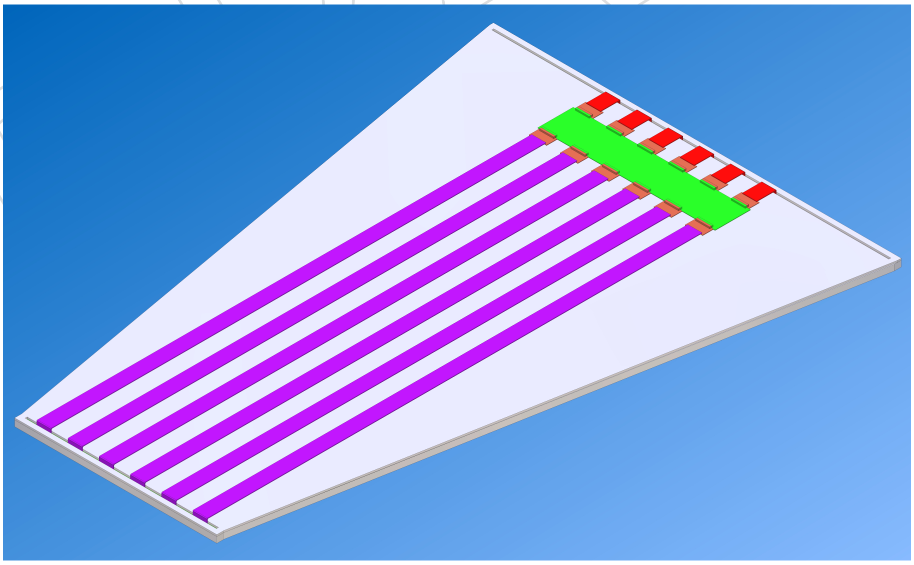

Figure 14: Scheme of the new electronic readout. The mezzanine is in green and the coaxial cables coming from the two ends of the strips (violet and red flat cables) are connected to the mezzanine through matching small orange cards. The detector and the strips-PCB are inside the cassette and not visible here

(full circles) presence of the gamma background. The rates, R_{clus} and R_{str}, at the WPs at a distance of 42 cm from the source were measured as about 0.82 and 1.5 kHz cm^{-2}. The shift of the WP at Th = 250 μV was measured as 100 V (1.6% in $\Delta V/V$) while the value at Th = 1,000 μV was 160 V (2.6% in $\Delta V/V$), which implies the importance of the low threshold for achieving a small sensitivity of the detector properties to the background.

In Fig. 18 are shown ε_μ and $< C_s >$ (left) and ε_μ and $P(C_s > 6)$ (right) for the 1.4-mm double-gap RPC at a fixed threshold value of 300 μV and under three difference gamma fluxes. The strength of the gamma flux impinging in the RPC was adjusted by the distance of the detector from the gamma source (triangles and squares measured at 38 and 28 cm, respectively) and by using a lead absorber (full circles measured with an absorption factor of about 2.5 by using a lead observer at 38 cm). The rates, R_{clus} and R_{str}, at the WP corresponding to the largest gamma flux yields were measured as 1.85 and 4.14 kHz cm^{-2}. The shifts of the WP obtained from the data labelled *'without gamma* (open circles) to the one from the data obtained with the largest gamma flux (squares) was evaluated as 350 V (5% in $\Delta V/V$).

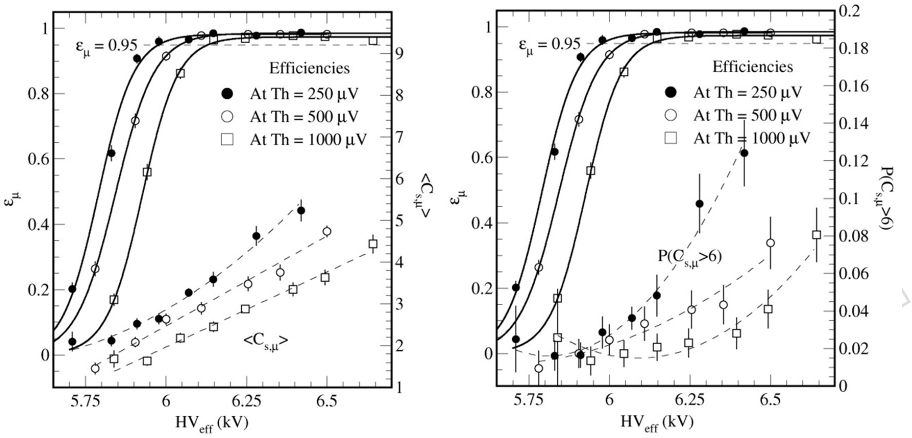

Figure 15: ε_μ and $< C_s >$ (left) and ε_μ and $P(C_s > 6)$ (right) as a function HV$_{eff}$ measured on the 1.2-mm double-gap RPC under a condition of no gamma background. The data measured at digitization thresholds of 250, 500, and 1,000 μV in the voltage-sensitive FEBs are labelled with the full circles, the open circles, and the squares, respectively.

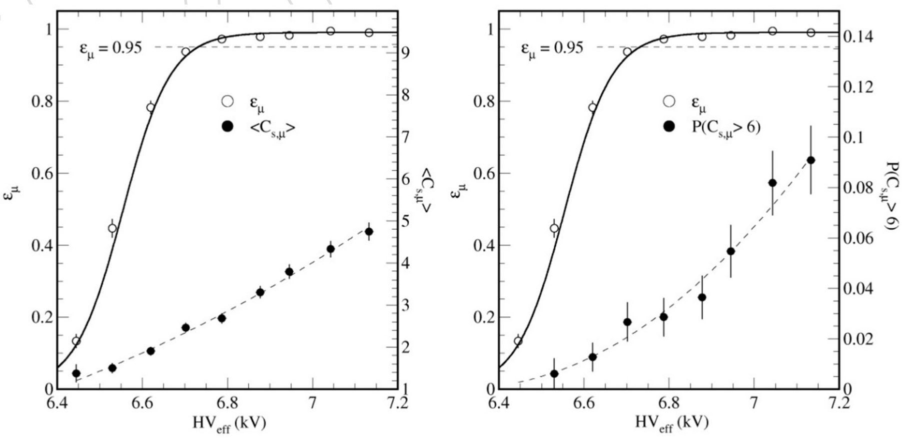

Figure 16: ε_μ and $< C_s >$ (left) and ε_μ and P(C_s >6) (right) at Th = 300 μV as a function HV$_{eff}$ measured on the 1.4-mm double-gap RPC under the same condition of no gamma background.

Reductions of the WP efficiencies due to the gamma background rates examined for the 1.2- (top) and 1.4-mm (bottom) double-gap RPCs are shown in fig. 19. The reductions of the efficiency at the rates of R_{clus} = 1.85 kHz cm^{-2} and R_{str} = 4.14 kHz cm^{-2} was measured as 2.92%.

As we increase the operational high voltage, the current per strip cluster drawn in the RPC approaches to the mean avalanche charge of the particle signal. The gain of the avalanche of a particle signal is reflected in its cluster size. In the middle of the muon efficiency plateau, the detector current per gamma strip hit is, therefore, approximately equivalent to the mean avalanche charge per strip hit.

Figure 20 shows the detector currents per gamma strip hit as functions of the rates measured for the 1.2- (left) and 1.4-mm double-gap RPCs (right). The data in the left figure for the 1.2-mm double-gap RPC, labelled with the full circles, the open circles, and the squares, were measured at Th = 250, 500, and 1,000 μV, respectively. The data in the right figure for the 1.4-mm double-gap RPC were obtained with the fixed threshold of 300 μV. As observed in the left figure in fig. 20, the decrease of the threshold value by the factor 4 leads to the reduction of a factor 2.4 in the avalanche charge per strip hit.

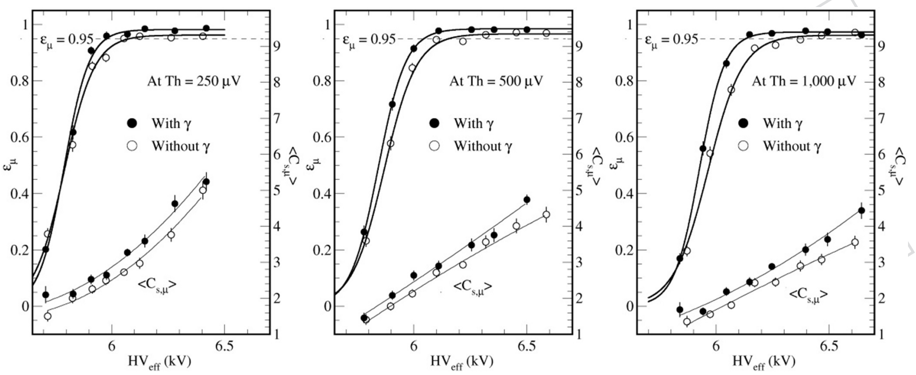

Figure 17: ε_μ and $< C_s >$ at Th = 250 (left), 500 (middle), and 1,000 μV (right) as a function of HV$_{eff}$, measured on the 1.2-mm double-gap RPC with (open circles) and without (full circles) presence of the gamma background.

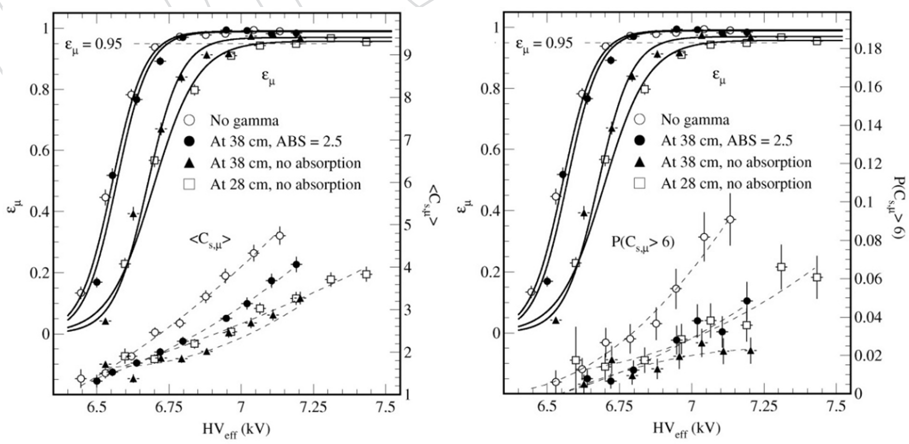

Figure 18: ε_μ and $< C_s >$ examined for the 1.4-mm double-gap RPC with a fixed threshold value of 300 μV and with three difference gamma fluxes. The details for the data symbols are described in the text.

We expect that the current that will be induced by the maximum particle rate of 600 Hz cm^{-2} (strip hit rate of $\sim$ 1 kHz cm^{-2}) in the future RE3/1 or RE4/1 RPC can be lowered to a level of about 70 μA m^{-2} when we lower the threshold from the current value of 160 fC to the level of 40 $\sim$ 50 fC (here, 250 $\sim$ 300 μV in the voltage-sensitive mode digitization).

The current R&Ds for RPCs in the proposed baseline design have been carried on the current tetrafluoroethane-based gas mixture for the CMS RPC operation (95.2% $C_2H_2F_4$ + 4.5% iC_4H_{10} + 0.3% SF_6).

The test results performed at GIF++ and KODEL, as shown in the previous three figures, prove the desired rate capability for the future CMS *i*RPCs. For intensive R&Ds to develop qualified detectors, we plan a series of beam tests on real-sized prototype RPCs developed with the proposed thin RPC model at GIF++ for coming two years from 2017, In addition to addressing the data quality at the high background condition, confirmation of the detector longevity is also critically essential.

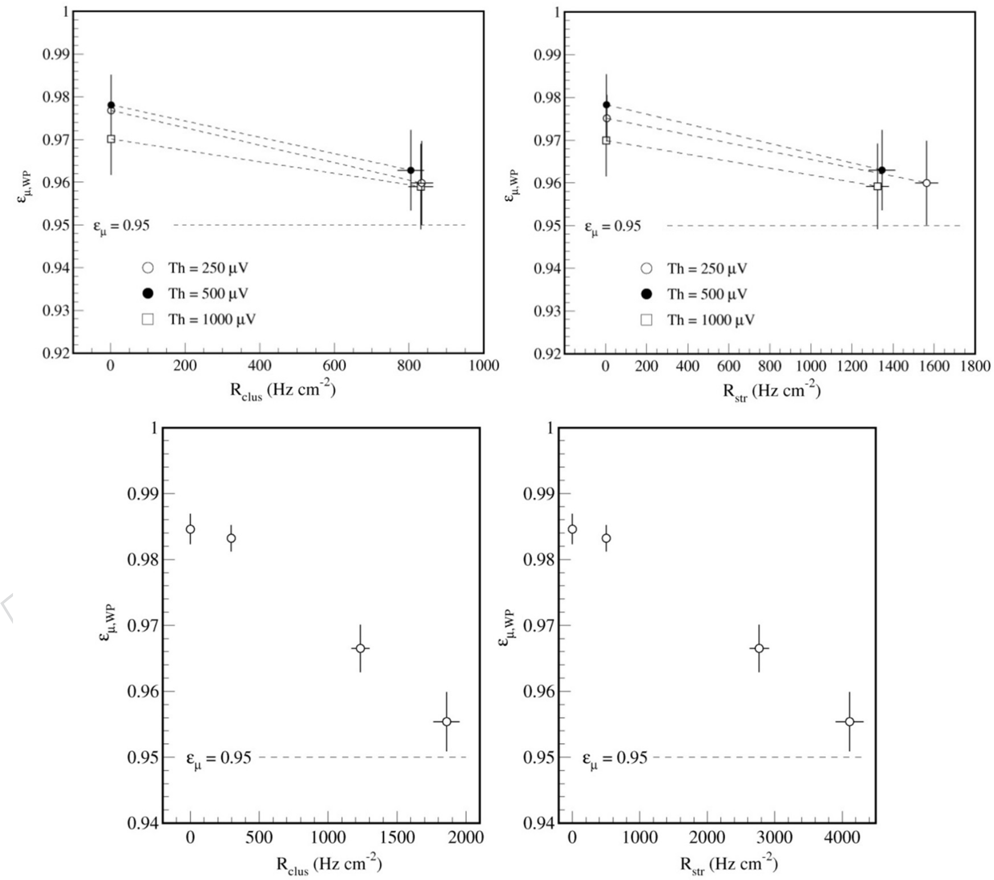

Figure 19: WP efficiencies at $R_{clus} \sim$ 0.82 kHz cm^{-2} (left) and at $R_{str} \sim$ 1.5 kHz cm^{-2} (right) measured for the 1.2-mm double-gap RPC in the top panels and for the 1.4-mm double-gap RPC as functions of R_{clus} (left) and R_{str} (right) in the bottom panel. The data for the 1.2-mm double-gap RPC, measured at Th = 250, 500, and 1,000 μV, are labelled with open circles, full circles, and squares, respectively. The data for the 1.4-mm double-gap RPC were measured at the fixed threshold of Th = 300 μV.

0.5.4 Technological aspects of bachelite detector production

0.5.4.1 Gas gaps

The important design parameters for the production facilities depends on the mechanical uniformity and the electrical stability of the gas gaps. In addition, the maintenance of initial detector characteristics for the long term CMS operation was also an important factor to be considered for the preparation of the detector production facilities[**?**].

- HPL Electrodes

  HPL panels for the RPC electrodes are cut, cleaned Puricelli and delivered to KODEL. A batch of qualified HPL electrodes produced for the previous RE1, RE2, and RE3 RPCs are shown in Fig. 21. Inspections of surface quality, measurements of the resistivity values, and selections of the qualified HPL electrodes are performed at INFN, Padova. After the delivery, the same visual inspections for the HPL electrodes are carried out at KODEL to ensure the qualification.

- Graphite coating

  Thin graphite layers both on the high voltage and on the ground sides of gas gaps are coated by a silk screen method. The surface resistivity of the graphite layer ranged from 100 to 250 k$\Omega/\Box$ after being dried for 5 days. The operation table and the accessories are shown in the left figure in Fig. 22.

- Insulation of graphite layers

  The graphite layers of the gas gaps were electrically protected by a 190 μm thick polyester (PET) sheet. Adhesive based on ethylene vinyl acetate(EVA) was utilized to glue the PET film on the graphite coated bakelite sheet. The thin film of the 'hot' adhesive was extruded through a long 500 μm wide slit, and was immediately dispensed over the graphite coated HPL surface. The extrusion facility and the control device of the PET film coating is shown in the right figure in Fig. 22.

- Gluing gaps

  Flat metric tables, rubber chambers for pressurization, specially machined jigs to fix the spacers and the peripheries were utilized to assemble the gas gaps (left figure in Fig. 23). Circular spacers and edge profiles, supporting a gas gap, were properly

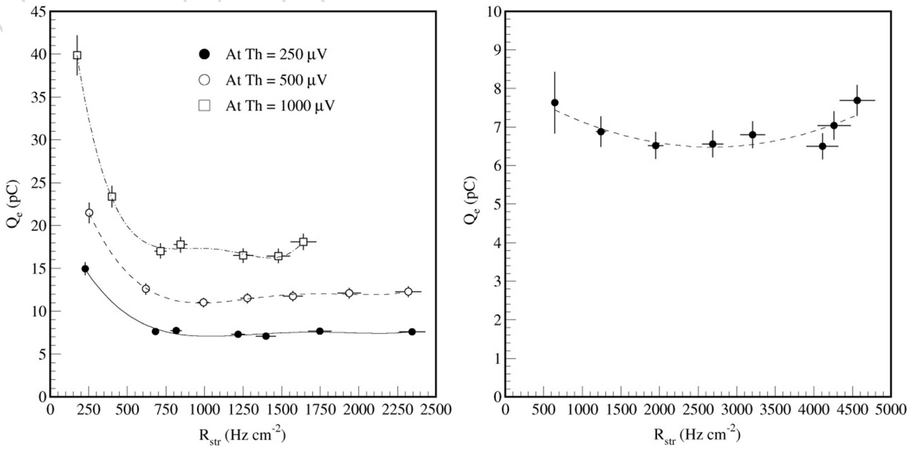

Figure 20: Detector currents per gamma strip hit as a function of Rstr tested for the 1.2- (left) and 1.4-mm double-gap RPC (right). The details for the data symbols are described in the text.

Figure 21: A batch of qualified HPL electrodes produced for the previous RE1, RE2, and RE3 RPCs.

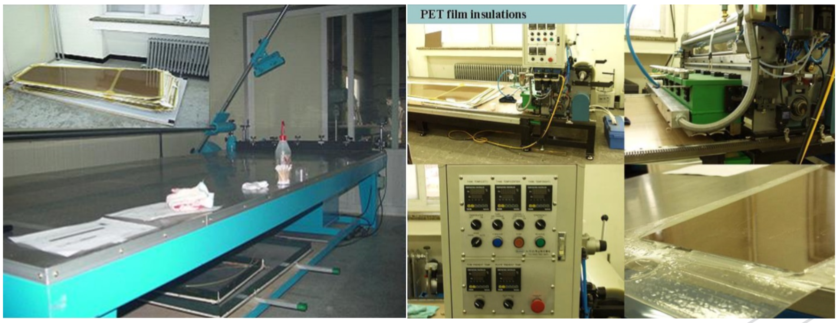

Figure 22: Operation table and the accessories of the graphite coating (left) and an extrusion facility and the control device of the PET film coating (right).

grinded to maximize the bonding strength with epoxy. Each flat metric table, where a few sets of gas gaps can be assembled, slided into a chamber for curing epoxy. The working time for the epoxy was 60 minutes, and the glue curing time to get the full strength of hardening was roughly 24 hours at 25 °C. During the glue curing time, an air loaded rubber chamber uniformly applied a positive pressure of 20 hPa over the whole surface of the gas gaps and the metric table.

- Oil coating

  The oil coating facility, shown in the right figure in Fig. 23, consists of two oil tanks, one lifting device, two air pumps, one air compressor, and a press device which vertically holds the gas gaps both during the oil coating and the air drying. The lifting device, holding a 200 l oil tank and moving up vertically with a constant speed of 2 cm per minute, hydrostatically injected the oil in the gas gaps which were mounted vertically in the pressing device. The air pump affected roughly 100 hPa to the gas gaps from outside so as to keep the pressure below 1 atm even after the oil was fully loaded. As the lifting device declined, the thin linseed oil layer automatically formed over the inside surfaces of the gas gaps. The expected thickness of the oil layer was $3 \sim 5\ \mu$m.

  Right after the drain and suction of the linseed oil from the gas gaps, air with relative humidity of 40 % was applied for drying the oil layers. The flow rate applied per a gas gap ranges from 70 to 100 l/h. The period of applying the air ranges from 40 to 60 hours The addition of humidity to the air was important to restrain any deformation of the gas gaps due to drying. The test results for a few samples, produced by this oil coating facility, to check condition of the polymerization of the oil layer is satisfactory.

- Tests for mechanical qualification (quality control step 1, QC1)

  Failure of spacers and the bonding strength, and a test for the gas tightness of the glue-cured gaps are performed by injecting a positive air pressure of 20 hPa to the gaps. In the previous construction of RE4 RPCs, any loss of the applied pressure

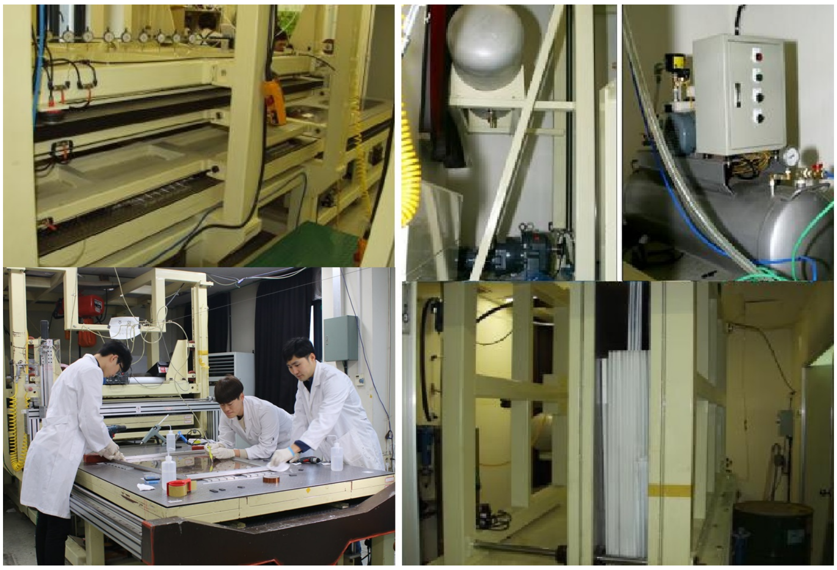

Figure 23: Flat metric tables, rubber chambers for pressurization, specially machined jigs to fix the spacers and the peripheries to assemble the gas gaps (left) and oil coating facility composed of two oil tanks, one lifting device, two air pumps, one air compressor, and a press device (right).

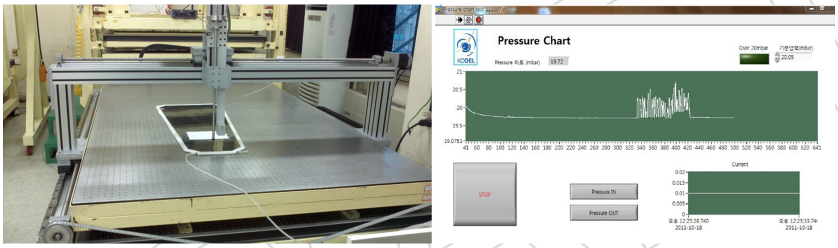

Figure 24: Test facility for the mechanical qualification composed of a metric table and a gantry arm equipped with a pencil-shape probe (left) and a pressure chart of testing the spacer failure and the gas tightness (right).

should be less than a threshold rate that are related the peripheral length of the gap and ranges from 0.15 to 0.4 hPa[**?**]. The test facility for the mechanical qualification is composed of a metric table and a gantry arm equipped with a pencil-shape probe, as shown in the left figure in Fig. 23. A pressure chart of testing the spacer failure and the gas tightness is shown in the right figure in Fig. 24.

- HV tests (quality control step 1, QC1)

  The qualification for high voltage is composed of three steps; an initial HV scan, a 120-h HV test at the working point, and a second HV scan to observe the change in the behavior of Ohmic currents. The gas mixture for the HV tests is composed of 95% tetrafluoroethane and 5% iC_4H_{10}. The criteria of ohmic currents selecting the qualified gaps will be decided in the phase of preproduction of the gas gaps.

0.5.4.2 Assembly of RPC modules

The qualified gaps produced at KODEL will be delivered to and assembled at 904 assembly laboratory at CERN. Quality control step 2 (QC2) pursues the objective of validating the RPC gaps performance repeating the test performed at KODEL in order to spot any damage that may haveoccurred during the gap transportation.

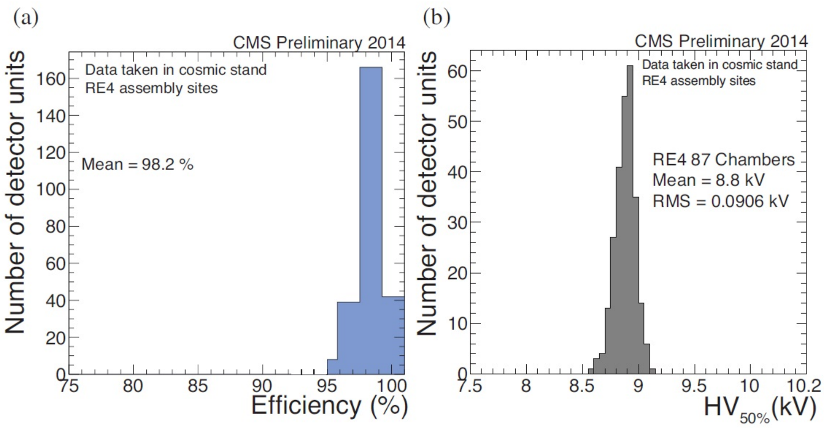

Figure 25: Mean cluster sizes (left) and working points (right) of the previous RE4 detectors performed with the cosmic muons in the QC3 step.

After a set of three gaps is fully validated at CERN, the chamber construction and commissioning begin. The quality control at the level of the chambers (QC3) foresees: chamber visual inspection, gas tightness, electrical and dark current measurement, cosmic muon commissioning by means of a dedicated cosmic ray telescope. The test results for the previous RE4 detectors performed with the cosmic muons in the QC3 step are shown in Fig. 25 (efficiencies on the left and working points on the right)[**?**].

After a successful cosmic test, every chamber is kept powered on and monitored for about three weeks in order to check its stability over time in the final step of the quality control (QC4). Some of RE3/1 and RE4/1 chambers will share the same cooling circuit and gas pipes, and be mechanically attached to the same structure. Then, an additional commissioning procedures are to be performed before the real detector installation at CMS.

0.5.5 Multigap RPC option

An alternative option to the HPL double-gap RPC is the Multigap Glass RPC (MGRPC) that would provide time resolution of the order of 100 ps and that has been verified to fulfill the needed rate capability expected during HL-LHC operations.

The proposed MGRPC layout prototype has five gas gaps of 250 m width. Low resistivity glass plates 0.7 mm-thick with the resistivity of about 10^{10} Ω·cm are used as electrodes. One glass with the dimension of 20 25 cm2 and another glass with the dimension of 27 25 cm2 are jointed together with a 0.5 mm-wide fishing line in the middle. The edge of electrode glass is not graphited in case of spark. This prototype consists of 12 double-ended readout strips of 17 mm width, 19 mm pitch.

0.5.6 Front-end electronics and DAQ for new detectors

0.5.6.1 Requirements

In order to reduce the amount of the avalanche charge associated to the passage of charged particles through the RPC without affecting the detector performance a new readout system equipped with low noise Front-End electronics able to detect lower charges without increasing the electronic noise is required.

The Front-End electronics need also to be fast-speed and robust to sustain the high irradiation environment that will prevail in RE3/1 and RE4/1 in the HL-LHC phase. The new available technologies that allow to minimize the chip size are thus to be used.

In addition, RPC detectors have fast timing capability. To exploit this feature to improve trigger and physics performance but also to better localize the clusters η position, it is important that the new FE electronics preserves the RPC signal quality and measures precisely its arrival time.

0.5.6.2 Electronic readout

Several ASICs with low-level noise able to read out the RPC detectors are available. One of these ASICs is named PETIROC (Figure 26). It is a 32-channel ASIC using a broad band SiGe fast amplifier and a fast SiGe discriminator. Its overall bandwidth is 1 GHz with a gain of 25. Each channel provides a charge measurement and a trigger output that can be used to measure the signal arrival time. It was originally developed by the OMEGA group [ref] to read out SiPM devices but its dynamic range (160 fC-400 pC) qualifies it for the readout of RPC detectors as well. Thanks to its low-jitter preamplifier the ASIC jitter is very small and goes below 20 ps for charges above 1 pC when in the absence of internal clocks as can be shown in Figure 27. To uniformise the 32 channels response the ASIC has two adjustment systems. A common 8-bit and an individual 6-bit DAC adjustment . Figure 28 shows the pedestals dispersion before and after the adjustment.

Although this ASIC was not developed for CMS, a new version, to be called CMS RPCROC, taking into account the CMS specifications is being worked out. In the new version the charge measurement will be dropped to simplify the ASIC and reduce its cost and power consumption. The charge could be still estimated using the TimeOverThreshold technique since the PETIROC ASIC allows the time measurements on both rising and falling edges. The ongoing development is common to the one being conducted by the same group to transform the SKYROC ASIC of CALICE into the CMS HGCAL ASIC and will hence benefit from the big efforts set by the CMS collaboration to achieve this[1]. Although the irradiation rate in the RE31 and RE41 is much smaller than the one to prevail int he HGCAL region the irradiation hardness of the new RPCROC ASIC should also get benefit of the HGCAL ROC development in this field. A change of the 350 nm SiGe technology used in the present PETIROC could be envisaged in case irradiation hardness is found to be not enough. Increasing the number of channels from 32 to 64 is also a possible option.

To read out the new RPC detectors independently of the final chosen technology (two-gap or multi-gap), a new Active Sensor Unit (a printed circuit board with electronics components on it - ASU) scheme using PETIROC (and ultimately the CMS RPCROC) is being worked out. The ASU will host pickup strips of 5-10 mm pitch, buried in a dielectric. The strips will be in principle as long as the RPC detectors. Both ends of one strip will be read out with two different channels of one PETIROC/CMS RPCROC. Thanks to the TDC precision of the order of 50-100 ps implemented in either an FPGA device externally or a chip internally to RPCROC, the precise information of signal time arrival from the strip's two ends will provide a precision on the coordinate along the strip length of the order of few centimeters.

The two strips ends will be rooted to the low eta, lateral edges of the ASU of the RPC chamber where two additional boards hosting each of them half of the RPCRPOCs and their associated TDC will be plugged. This structure is an advanced version of the one previously proposed (Figure 29, left) in which the ASICs and the TDC are set on the outer radius of ASUs. This scheme was abandoned due to constraints from the present RE3/2 and RE4/2 Endcap RPC stations structure.

[1] The dynamic range of the CMS HGCAL ASIC is not very well adequate for low charge signal otherwise one can envisage to use it to read out the CMS RPC detectors.

A medium size ASU with the previous scheme was designed as a demonstrator and then realized (Figure 29, right). The demonstrator hosts two 32-channel PETIROC ASICs as well as two TPCs implemented on a FPGA. The TDC, developed by the Tsinghua University, uses delay-path based techniques. The TDC was adapted to have 32 independent channels that receive each the trigger output of one of the 32 PETIROC channels. The same FPGA used to host the TDC is used to configure the ASICs thanks to a dedicated firmware that provides also the needed state machines that enable recorded data to be properly ordered in time. First tests on the demonstrator have shown that a timing as good as 30-35 ps can be achieved (Figure 30) by

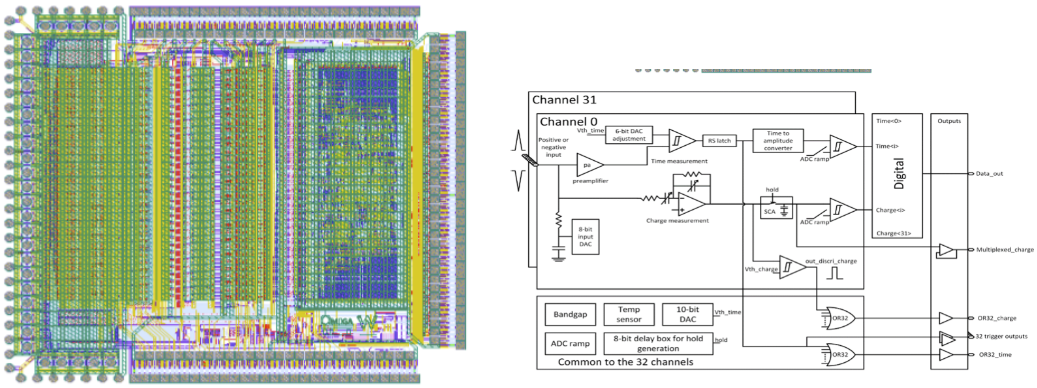

Figure 26: The PETIROC ASIC (left) and its schematics (right).

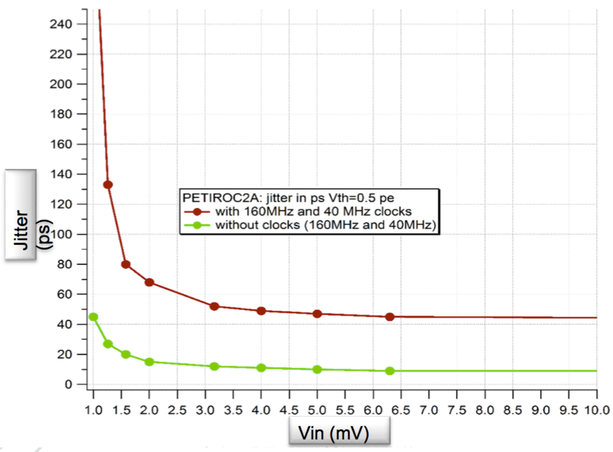

Figure 27: The PETIROC time jitter measured with and without clocks.

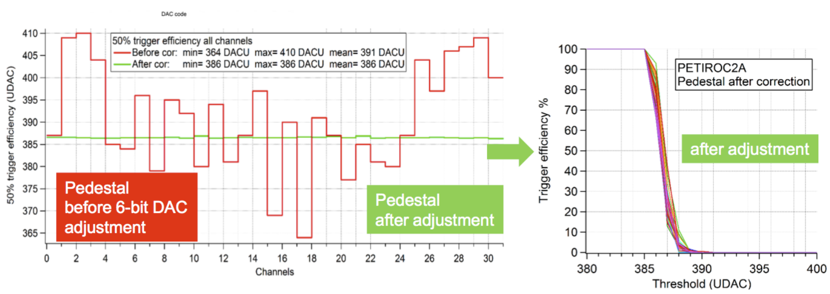

Figure 28: The PETIROC time jitter measured with and without clocks.

measuring the difference of time arrival of the signal by two of the TDC channels associated to the two ends of the same strip after an injection of a 10 pC on test points places on the path of each of the strips.

To get the same response of the different ASIC channels to the same injected charge, the individual threshold of each of the channels was fixed in such a way that their pedestals have similar values. This results in similar S-Curves (Figure 31). A system allowing the synchronizing of the different TDC channels was also developed and implemented as well as an external trigger system. The ASU was used to read out one of the current CMS RPC gap (2 mm gas gap enclosed between two HPL plates of 2 mm thickness) on a test bench (Figure 32, left) equipped with three Scintillator-PM devices producing an external. triggering signal when a charged particle crosses the. Albeit the some-how large thickness of the dielectric layer used to burry the strips, the results obtained with the demonstrator ASU are excellent. An efficiency as high as 94% is obtained and a time resolution of 230 ps is measured (Figure 32, right). This includes a 100 ps resolution due to the spread induced by the scintillator surface overlap of 5 cm$\times$ 5 cm used in this study. This is a very good result taking into account the absence of Faraday cage protection and the fact that only one rather two gaps are used with smaller induced charge due to the dielectric thickness. It allows the determination of the hit position of better than 2 cm along the strip direction.

0.5.6.3 DAQ layout

Each of the two stations RE3/1 and RE4/1 is made of 18 detectors (20° span). As mentioned above, each strip will be read out thanks to two channels associated to the two ends of the strip.

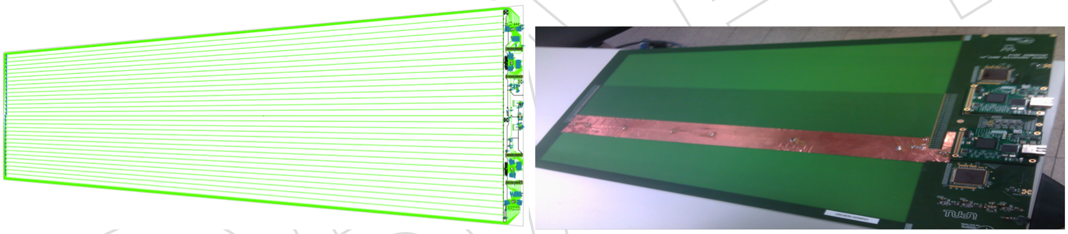

Figure 29: Left: Schematics of a large ASU with pickup strips read out from both ends by two independent channels of the the same PETIROC. ASICs and TDC on FPGA mezzanines are placed on the outer radius. Right: a picture of a realized medium size ASU following the same schematics with pickup strips in the middle.

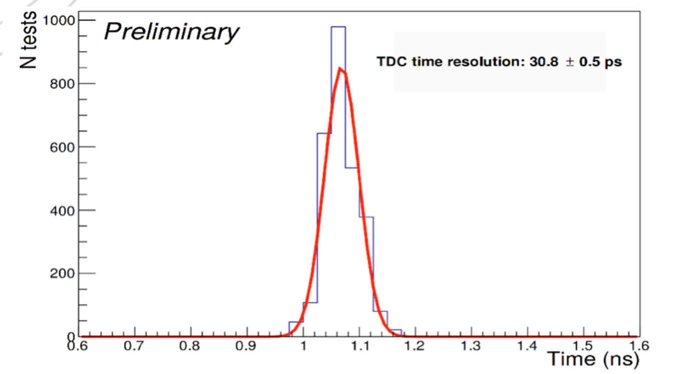

Figure 30: Time resolution of the arrival time difference of one of a signal of 10 pC injected on one of the ASU's strip.

Signals above a given threshold will be recorded and their time arrival will be measured thanks to the TDC. The TDC will be either on FPGA device or embedded in the RPCROC chip.

An expected maximum of 2 $\times$192 channels (6 ASICs of 64ch) are needed to read the strips of one detector leading to 6912 channels for each station. Each detector will be equipped with a dedicated board that collects the data coming from the FE of one detector and then transmits it either directly to the MFT (18 optical fibers needed) or to a data concentrator as an intermediary step before the MFT if the number of available input of the MFT does not allow to receive all these fibers. Figure 33 represents the schematics of the expected DAQ structure.

There are 4 dedicated DAQ boards, two for each End-cap. Each optical link coming from one chamber is split in two and connected to two different DAQ boards. The splitting of the optical links and the use of two DAQ board rather than is intended to ensure the system redundancy. Two reconstruction levels are to be run on this board before any data being transmitted to the global muon trigger or to the central DAQ on L1A signal. First, the time measurements on each end of the strip are combined to compute the position in Y along the strip (difference compatible with the strip length) and the delay to the bunch crossing (mean time arrival). The computed positions (chamber, strip,Y, time) are buffered waiting an L1A signal to be transmitted to the central DAQ. Then, the hits compatible in time and geometry between the different chambers and station are combined to provide hits and track segment candidates to the global muon trigger system where they are compared withe information of the CSC of the same sta-

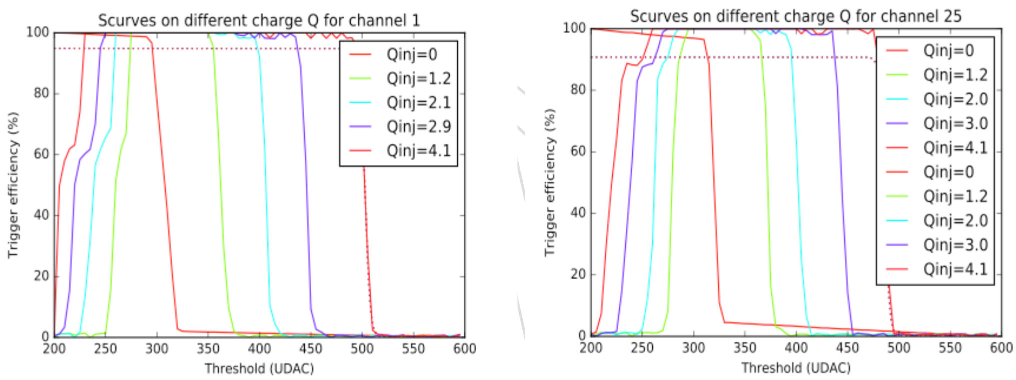

Figure 31: Time resolution of the arrival time difference of one of a signal of 10 pC injected on two of the ASIC's channels .

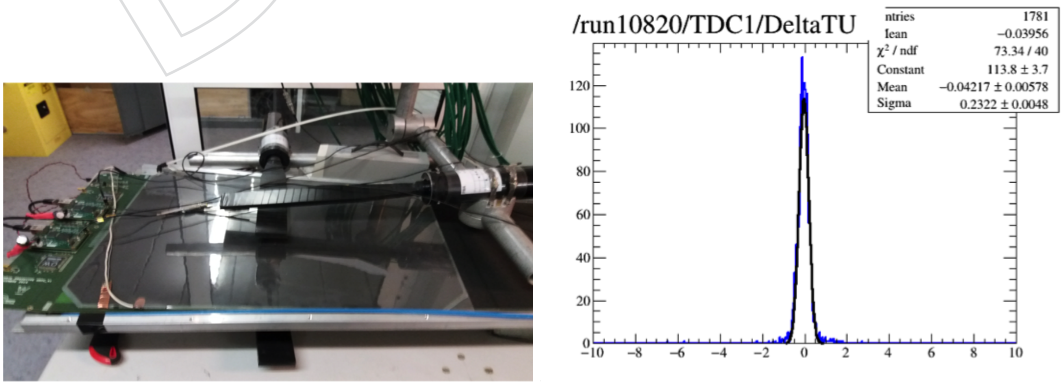

Figure 32: Right: Cosmic bench to test the RPC gaps. Left: time resolution of the time difference $T_2 - T_1$ of 24 of one of the TDC channels.

tions.

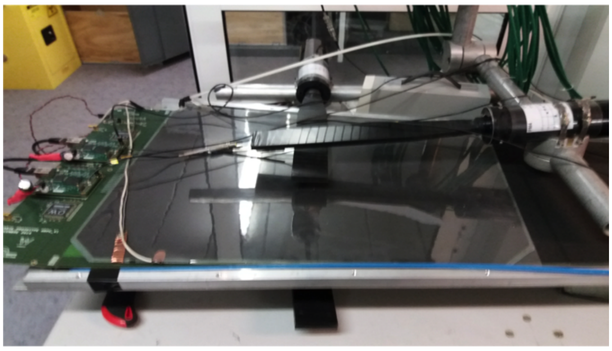

Figure 33: A schematic of the new DAQ system.

The data to be transmitted should include a header that contains the station information (RE3/1 or RE4/1), the detector number (from 1 to 18), that of the FE ASIC (1 to 6) and the channel number (1 to 64) to determine the position of the each strip and which readout end. The header is followed by the information of the time of the detected signal of each channel. The time should be coded in 12-14 bits. It is possible to have two time information (signal falling time in addition to the rising one to be used in the TOT protocole).

We expect at most 2 KHz/cm^2 (it is 600 Hz/cm^2 but we take a safety factor of 3). This leads to 0.36 $\times 10^{-2}$ hits/channel every 25 ns. This results in about 0.36 $\times 10^{-2} \times$ 4 byte $\times$ 6912 $\leq$ 0.12 kByte every 25 ns to be transmitted by each station (4 byte per signal is estimated including the two time information). For the 72 chambers of the 4 stations this amounts to about 4.2 Gbytes/s of data rate to be transmitted.

0.5.7 Installation and integration

0.5.7.1 mechanical aspects

The RE3/1 chambers will be mounted on the YE3 steel as shown in the figure 34. They will overlap the circular (18 Trapezoids) neutron shielding attached to the YE3 and reaching the cylindrical neutron shielding surrounding the collar that separates the yokes YE2 and YE3.

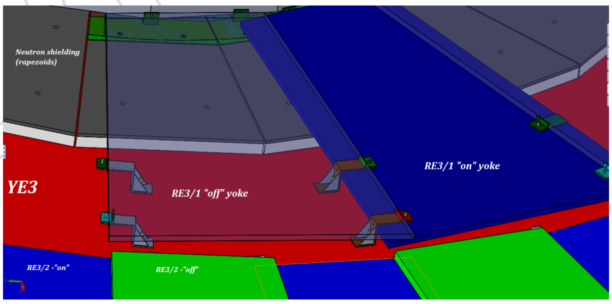

Figure 34: Schematic view of the mounting of RE3/1 chambers on the YE3 steel plate.

The chambers will be mounted directly to the yoke. Using the foreseen M12s threaded into the yoke steel. Allowance for sagitta in the yoke will be made using a simplified kinematic mounting. The screws and washers securing the neutron shielding will be modified to make them flush with the lead part of the shield so increasing the available space in Z.

For RE4/1 the mounting is quite different as they mount to the same yoke as the ME4s taking advantage of the CSC mounting posts which will be extended with large M24 studding. To these supports will be built a thin light weight frame made from aluminium alloy 8mm thick. The chambers are then screwed to this frame.

Access for both chamber installation and commissioning will necessitate the *push back* of the YE4 from the YE3. The negative end has been already used but the positive end has yet to be commissioned. The schedule dictates that services will be installed prior to the LS2 during the EYETS. During the LS2 all other works. [Show that the mounting is feasible as it is identical to the RE4/2 and RE4/3 SMs already installed]

0.5.7.2 power system

The High Voltage power system for the new Chambers will be a copy of the actual system. The High Voltage power modules CAEN A3512N will be installed in the present USC RPC HV racks. This will necessitate the installation of 4 more umbilical cables from the USC to the UXC connecting via the YE1 Patch Panel (PP). From the main YE1 HV PP, where there is space in the present panel, the single channel cables will go through the Mini Cable Chains (MCC) to the YE3 where they will be distributed around the peripheral cable trays.

For what concerns the Low Voltage (LV) system, optimisation of costs dictates that the same Easy crates and LV modules (CAEN A3016) already in UXC will be used to power the new chambers. Re-cabling in front of the LV modules will be done in order to liberate the two modules required. Service Power and Communication bus for these crates, through the A1676A Branch controllers, is done from the USC X4F03 rack.

Space in the USC S1F06 rack will be used for the trigger system.

[Do we need a table with number of HV and LV modules ?]

0.5.7.3 UXC and USC Rack space

The racks on YE3 are largely occupied. Space is required for the LV system, DCC and associated FO patch panels. The two RPC gas racks are on X2 Far. The RE3 rack has sufficient 12 spare channels for the RE3/1 and RE4/1 chambers with 1 channel per 60 degrees.

Additional racks space is required for the HV and Data/control functions in the USC. The LV system is controlled through the A1676A modules presently located in the X4F03 rack in the USC. The Trigger system including Fibre optic cable patch panels will be required in the Trigger racks in the USC. Additional racks will be required adjacent to the S1F01 to 05 racks. Space is available in S1F06 adjacent to the present Trigger system. If necessary space is also available in a rack (S1F00) closer to USC.

0.5.7.4 readout system

The data and control from the chambers is achieved by fibre optics rather than by copper cable. Given the few channels required for this Fiber Optic cables can be installed by hand as per the Trigger LB system in two of the six channels between USC and UXC.

0.5.7.5 cable routing

Trials have been performed to show that both cable and piping services of RE3/1 can be routed between the Yoke and rear face of the chambers both of which are smooth uninterrupted surfaces. This solution is preferable to installing services over the top of the presently installed RE3/2 and RE3/3 chambers as this would hinder the access and removal of same. Running these services behind the chambers will require prior installation to the chambers, meaning that installation should be done during the preceding EYETSs.

Although the job is more fastidious the RE4 SMs will remain in place which is far better than disconnecting all the services and removing all the chambers. The CSC electronics will be changed, scheduled to coincide so that the services will be mounted over the CSCs in ducts and secured to the RPCs. Services will be routed between the CSC and RPC chambers where there is plenty of space. Specific cabling specification is required to ensure the RPCs do not create noise problems for the CSCs. More care will be taken by passing the services through ducts and to mount cable and pipes to ensure that we are within the RPC volume given by the RE4 SMs.

Fig. 35 shows the space available for RPC services between CSCs and RE4s chambers.

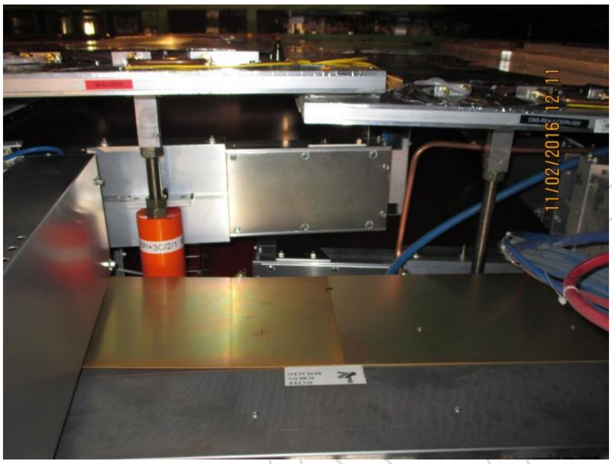

Figure 35: Picture showing the available space for RPC services between CSCs and RE4s chambers.

Although the mini cable chains a quite full the near side chain has sufficient space for the HV and Fibre optic services to transit here. The 2 umbilical HV cables and Fibre optics will fit in the main cable chains. The Main cable chain is extremely full. The need for 2 umbilical HV cables in each is xxxxx cm^2.

For mini cable chains, altough they are also quite full, the near side chain has sufficient space for the services to transit there.

Optical fibres will go through the two FO passages leading to the base of the Main cable chains in the UXC as there is enough space for them.

0.5.7.6 gas and cooling system

The gas mixture is identical to the present system. The only modification will be after the UXC distribution racks. New piping and patch panels will have to be installed around the yoke on non IP side of the yoke for RE4/1. The presently installed piping foreseen for RE3/1 will have to be modified as it used all 12 channels on the rack. The PP are in position on the yoke periphery. Their mapping will need modifying.

Table 1 shows the gas volumes and flows rates for the RE3/1 and RE4/1 chambers.

The cooling system specification is a function of the electrical power distributed into the UXC cavern. Technical Coordination have requested that all electrical load be cooled, meaning that

Table 1: Expected gas volumes and rates for the new RE3/1 and RE4/1 chambers

Endcap	Volume [l]	exchange rate/hour	Chambers per sector	flow rates per channel
RE3/1	4.5	1	3	13.5
RE4/1	3.5	1	3	10.5
RE3/1 station	81	1	3	81
RE4/1 station	63	1	3	63
Rack				144
Total	288			288

the minimum heat load should go into the cavern ventilation system. The chamber loads are significantly less than in the previous RPC chambers. Nonetheless the chambers and rack elements will be cooled by circulating water from the Endcap cooling circuit. The relatively small load can be accommodated by an extension of the present system.

Table 2 shows the expected power dissipation for the PetiRoc electronics with TDC integrated.

Table 2: Expected power dissipation for PetiRoc with integrated TDC for RE3/1 and RE4/1 Chambers

Channel	Chambers	1 station	1 YE3	Rack Power	PetiRoc dissipation
	640	18		86 %	
[mW]	[W]	[W]	[W]	[W]	[W]
6	3.84	69.12	138	119	514
	DCC per 6 chambers	1 station	1 YE3	Rack Power	DCC Dissipation
	40	120	240	206.4	892.8
Total					1407

This value of dissipated power is approx. 10% of the total power dissipated on both YE3s. This power should increase the coolant temperature by approx. 0.1 C°. Given the fragility of the cooling circuits on the RE4 SMs separate cooling circuits will be taken off the present *mini manifold* using tee connections and flow restrictors to equalise the flow in these parallel circuits (see figure 36).

The RE3/1 chambers will be cooled by extending the RE3/2 chamber cooling piping.

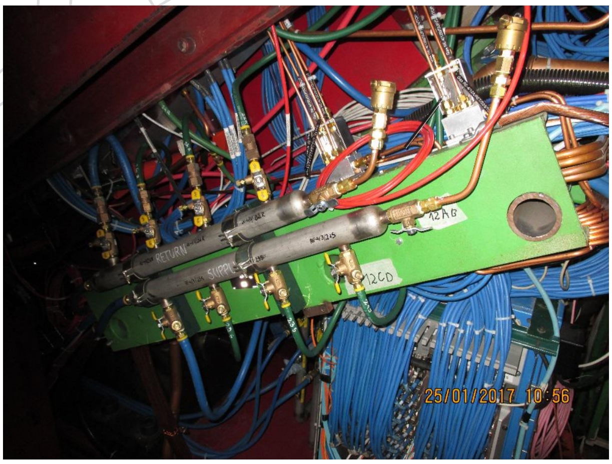

Figure 36: Proposed scheme for the RE3/1 extended cooling system.

0.6 Costs, Schedule and institutional responsabilities